REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
		FINAL REPORT 15 Sep 93 - 30 Apr 96

4. TITLE AND SUBTITLE
High Density Low Power RTD/HBT and RTD/HFET Technologies for High Speed Computing

5. FUNDING NUMBERS
A323/00
61101E

6. AUTHOR(S)
Dr K. C. Wang

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Rockwell International Science Center
1049 Camino Dos Rios
P O Box 1085
Thousand Oaks, CA 91358

AFOSR-TR-96
0519

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NE
110 Duncan Avenue Suite B115
Bolling AFB DC 20332-0001

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
F49620-93-C-0065

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE: DISTRIBUTION UNLIMITED

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

This program is directed towards the monolithic integration of resonant tunneling diodes (RTDs) and conventional heterostructure transistors, and the demonstration of high speed, low power, high functional-density circuits. This effort was carried out in close collaboration with MIT Lincoln Laboratory (LL). This team demonstrated lattice mismatched InGaAs/AlAs RTDs with high peak to valley current ratio (PVCR) and high current density capability, integrated with AlGaAs/Ga-As-based heterojunction bipolar transistors (HBTs) and hetero-structure field effect transistors (HFETs). We explored by simulation and experiment several novel digital integrated circuit approaches, based on this technology.

14. SUBJECT TERMS			15. NUMBER OF PAGES
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	

SC71088.FR

High Density Low Power RTD/HBT and RID/HFET

Final Report

Contract No. F49620-93-C-0065

ARPA No. A323

Prepared for:
AFOSR/NE
Directorate of Physics and Electronics
110 Duncan Avenue, Suite B115
Bolling AFB, DC 20332-001
Attn: Dr. Gerald Witt

Prepared by:
P. Zampardi and K.C. Wang
Rockwell Science Center
1049 Camino Dos Rios
Thousand Oaks, CA 91360

P. Asbeck
UCSD
9500 Gilman Avenue
La Jolla, CA 92093

October 1996

Rockwell

Science Center

Copy # 6

Table of Contents

List of Figures

List of Figures (Cont'd.)

1.0 Executive Summary

This program is directed towards the monolithic integration of resonant tunneling diodes (RTDs) and conventional heterostructure transistors, and the demonstration of high speed, low power, high functional-density circuits. This effort was carried out in close collaboration with MIT Lincoln Laboratory (LL). This team demonstrated lattice mismatched InGaAs/AlAs RTDs with high peak to valley current ratio (PVCR) and high current density capability, integrated with AlGaAs/GaAs-based heterojunction bipolar transistors (HBTs) and hetero-structure field effect transistors (HFETs). We explored by simulation and experiment several novel digital integrated circuit approaches, based on this technology.

Key circuits that have been designed are a 64-bit static RAM with HBT driving circuitry and RTD/HBT bit cells, resonant integrated injection logic (RI^2L), prescalars and logic gates, and resonant emitter HBT logic (REHL) full-adder, 2x2 multiplier circuit, and logic gates. A large number of test structures were also assembled to investigate issues such as device scaling and to further define design rules. These structures and devices have been assembled into a dedicated 14-level mask set for this program. Simulation of circuits using integrated HFETs and RTDs has been completed. A second mask set was assembled to study resonant direct-coupled FET logic (RDCFL), a logic family using RTDs as loads and FETs as switches; and RTD/HFET register logic (RRL), a shift register based logic using both RTDs and FETs. The key circuits are small RAMs, frequency dividers, and shift registers. Several wafers using this mask set have been processed.

Important milestones achieved on this program include: 1) fabrication of RTDs by Rockwell using material supplied by Lincoln Laboratory, 2) demonstration that HBTs are not severely affected by the RTD overgrowth/processing, 3) demonstration of RTDs and HBTs in the same wafer field, (The latter two accomplishments represent the first time that lattice mismatched RTDs on HBTs have been demonstrated.) 4) development of low In concentration HBT contact layer for reduced emitter resistance and improved morphology, 5) demonstration of

NAND, NOR, and Inverter logic gates in lattice mismatched HFET/RTD technology. (This is the first time lattice-mismatched RTDs co-integrated with HEMTs have been demonstrated.)

PROGRAM HIGHLIGHTS

- Verified that HBT layers did not degrade during RTD growth cycle.
- Fabricated RTDs at Rockwell using RTD material supplied by Lincoln Labs.
- Designed and simulated the following circuits:

  RI^2L: Multiple Fanout Gate, 17-Stage Ring Oscillator, 13-Stage Delay Chain, and frequency divider.

  REHL: Full Adder, Multiple Fanout Gate, 17-Stage Ring Oscillator, 13-Stage Delay Chain.

- Lincoln Laboratory (LL) has demonstrated a PVCR=9 lattice mismatched RTD on AlGaAs/GaAs HBT epilayers; subsequent HBTs were good.
- 1.5x1.5, 2x2, 1.4x3, 5x5, and 3x1.4x8.5 μm^2 RTDs have been demonstrated on HBT epilayers at Rockwell Science Center. The PVCR was 5, using material provided by LL.
- Demonstrated AlGaAs/GaAs HBTs on the same wafer as RTDs.
- Small area RTDs and HBTs have been demonstrated in the same wafer field with an RTD PVCR=9.
- Good emitter resistance with low In concentration cap layer demonstrated.
- AlGaAs/GaAs RTDs have been demonstrated on E/D HEMT Material.
- Design, simulation and layout of circuits for RTD/HEMT mask were completed, including shift-registers, small RAMs, logic gates, frequency dividers, and ring oscillators.
- HEMT/RTD Logic Gates using lattice mismatched RTDs have been demonstrated.

2.0 Material Development

Although Rockwell's HBT and HEMT processes are well-established, the integration of RTDs with these technologies raises several challenging material related issues. In collaboration with Lincoln Lab, we have demonstrated that questions related to lattice mismatch and thermal issues can be overcome, but need further refinement for circuit fabrication.

The first experiment was to have Lincoln Lab grow lattice matched AlGaAs/GaAs RTDs on AlGaAs/GaAs HBT wafers to determine the effect of the RTD growth (thermal cycle and process) on the HBTs. These HBT wafers did not have an emitter contact layer (InGaAs), which we will discuss later. The RTDs were deposited on these wafers, and large area HBT (67x67 μm^2) devices were then fabricated (by removing the RTDs then fabricating the HBTs with Rockwell's QuickLot process) and tested. The resulting Gummel plots are shown in Fig. 1a and b. The 550°C growth had very little effect on the HBT, while the 600°C growth had a substantial impact on the base current of the HBT. Since the lattice mismatched InGaAs/AlAs RTDs we intend to use for this technology are grown at 510°C, we expected very little degradation of the HBT due to the extra growth steps.

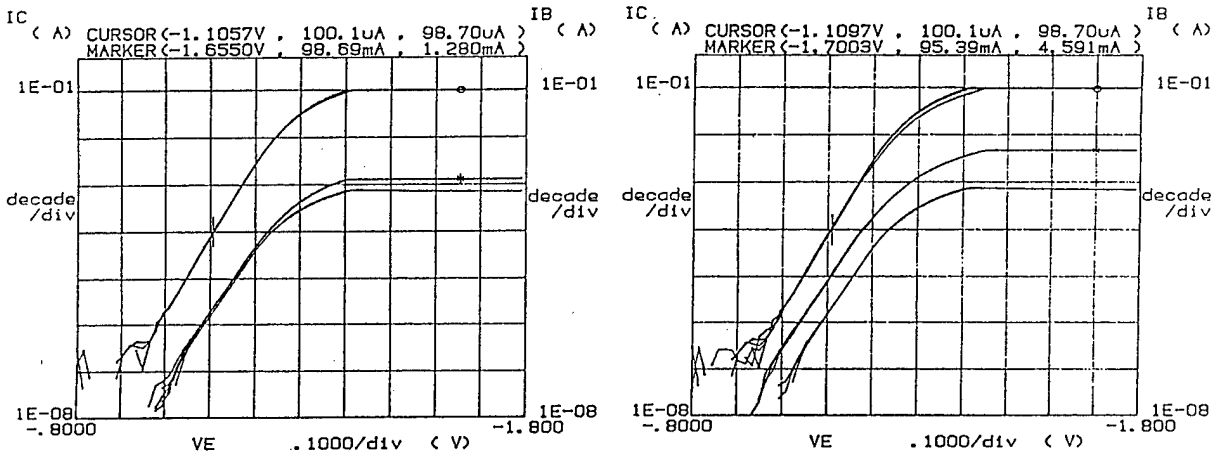
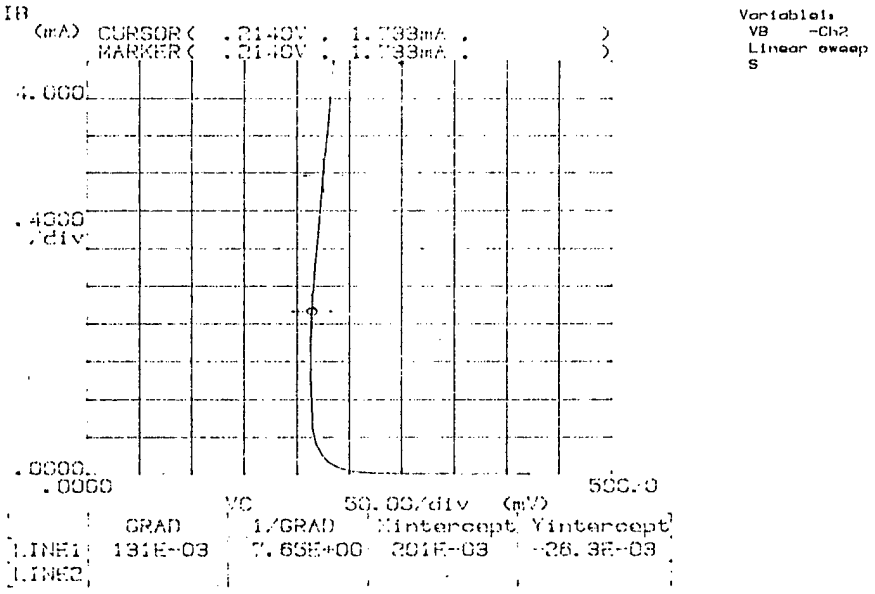


Fig. 1 a) HBT Gummel plot after 550°C, 1-hr RTD growth; b) HBT Gummel plot after 600°C, 1-hr RTD growth. Gummel plots of HBTs that have undergone RTD overgrowth. The RTDs for this program are grown at 510°C, so no difficulties associated with thermal cycle were expected.

We next provided LL with HBT material containing an InGaAs cap layer on the HBT emitter (for lower contact resistance). The estimated indium fraction at the top of the cap layers was 50%, and the surface quality of the material was rather poor because of the large lattice mismatch to the GaAs below. As a control sample, LL first grew an $In_{0.53}Ga_{0.47}As$/AlAs RTD directly on the InGaAs cap without any buffer layers. The result was an RTD having a PVCR of about 2.5 at room temperature. This is compared to a PVCR of about 10 for the same InGaAs/AlAs RTD structure lattice matched to InP. LL is quite sure that the degradation was caused by surface roughness and not dislocation density. Growing directly on the InGaAs cap is problematic because molecular beam epitaxy is not effective at smoothing an already rough surface. The surface roughness at the top of the HBT InGaAs cap layer is substantial enough to increase the valley current of any subsequently grown RTD. It is, perhaps, a testament to the quality of the LL InGaAs/AlAs RTD that a PVCR of 2.5 was obtained rather than no PVCR at all.

Removal of this cap layer solves the surface morphology problem, but creates the problem of high emitter resistance that seriously affects both the device and circuit performance. The effect of this emitter resistance is particularly detrimental for the REHL logic family, since it causes the circuits to oscillate. For this technology to be realized, a material structure/process that provides good surface morphology while at the same time providing low contact resistance to the HBT emitter must be developed. A low indium concentration cap layer with an alloyed emitter contact meets both the criteria for surface roughness and low contact resistance. We have demonstrated that In concentrations as low as 10% still provide excellent emitter resistance and have a much better surface morphology than the higher indium concentrations. A measurement of the emitter resistance by the flyback method on one such wafer is shown in Fig. 2. An additional concern was the fact that the original RTD/HBT buffer was undoped. Changing this to doped InGaAs relieves some of the etching tolerance in etching from the RTD mesa layer to the HBT emitter.

FLYBACK QT1 MBE 261



RE = 7.652

Fig. 2 Flyback measurement of emitter resistance on 1.4 X 3 μm^2 HBT with low doped Indium cap layer. (After removal of RTD layers.)

Since HEMTs are grown under similar conditions to the RTDs, there was very little concern about the material issues, other than the lattice mismatch. The only special consideration was the addition of an etch-stop above the HEMTs so that the etching from the RTD layers to the HEMTs was controllable and repeatable. However, the same morphology issues discussed above apply to the RTDs grown on HEMTs as well. Excellent HEMT characteristics were obtained with both lattice matched and lattice mismatched RTDs. Typical HEMT characteristics are shown in Fig. 3.

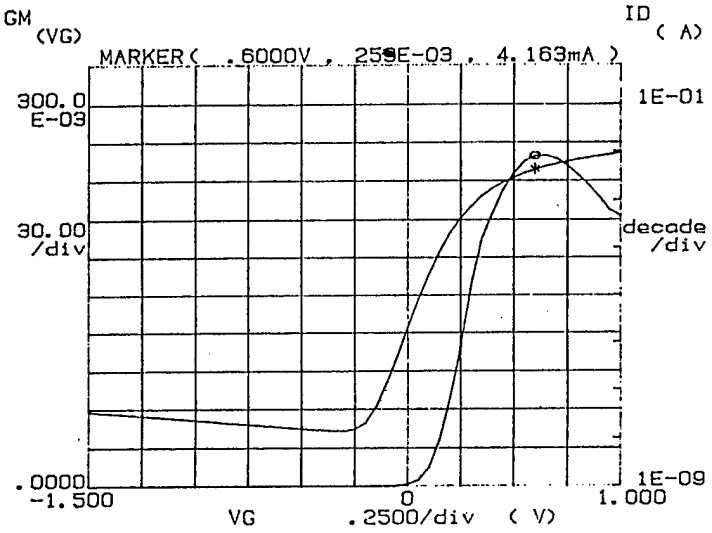


Fig. 3 HEMT I_d vs V_g curve and transconductance — Peak transcunductance is 259 ms/mm for this is 50 μm FET.

In summary, this collaboration has demonstrated that many of the key materials issues can be overcome. Excellent emitter resistance and surface morphology can be obtained with low In concentration cap layers, and lattice mismatched RTDs with good peak-to-valley-current ratio can be fabricated on AlGaAs/GaAs HBTs without degrading the HBT. HEMTs with excellent characteristics were demonstrated with the lattice mismatched RTDs. The demonstration of this material integration is critical for this technology and illustrates that such integration of quantum devices and conventional transistors, although difficult, is achievable.

3.0 Process Development

3.1 RTD/HBT and RTD/HEMT Process Development

Several key elements of processing technology were developed for this project: 1) the ability to remove the RTD layers exposing the emitter contact layer for the HBT or HEMT, 2) the fabrication of small area RTDs on top of a tall mesa to accommodate the buffer layer between the RTD layers and the HBT or HEMT layers, 3) the development of an interconnect process

that will handle the steps over the various mesas used, and 4) the development of an emitter contact that is compatible with the RTD regrowth while still maintaining low contact resistance (which results in low R_{ee}) for the HBT.

3.2 HBT Development

The HBT process used for this project is well-developed and was transferred into a manufacturing facility before this program began. It features implants to isolate both the base and collector regions. This is not as effective as our SADAP (Self-Aligned Dielectric Assisted Planarization) for reducing C_{bc}, but for this application the speed of the HBT was traded for improved planarity (which results in higher yields). A similar process is used in Rockwell's BiFET process, which combines HBTs with MESFETs[1]. However, the emitter contact layer needed to be modified to accommodate the overgrowth of the RTD. The InGaAs contact layer typically used on Rockwell's HBTs has a $In_{0.5}GaAs$ layer 400Å thick. Since this layer has a large lattice mismatch to GaAs, the surface morphology is very rough and not an acceptable starting point for the RTD regrowth. The first attempt at a suitable contact layer was to remove all the Indium and dope the GaAs layer as high as possible. Unfortunately, our material vendor uses Si as the n-type dopant and 5×10^{18} cm^3 is the highest doping level that could be obtained. Ohmic contacts to this layer proved marginal and resulted in higher (>50 ohms for a 1.4 x 3.0 μm emitter) R_{ee} than is acceptable for good device/circuit performance. We then tried adding 10% indium to this layer to decrease the contact resistance while maintaining a good surface morphology for the regrowths. This particular process does not allow for the fabrication of emitter contact TLM, and funding and time constraints did not allow for the processing of test wafers, so the results for these wafers were not available. Thus, this experiment was carried out on actual RTD/HBT wafers in which the RTD layers had been removed and HBTs fabricated. The R_{ee} of a 1.4 x 3 μm^2 emitter was much improved, with the emitter resistance now between 30 and 50 ohms. The effect of emitter undercutting or over etching of the etch stop layer on is not known for these results. A serious constraint of using an InGaAs contact layer is that this

layer still needs to be very thin, <1000Å, for the HBT. This leaves little room for a cleanup etch (over etch) when the RTD layers are removed. The next step in developing this layer would be to implement tellurium (Te) as the dopant for a GaAs contact layer so the doping level can be increased without the use of indium. Once this is successfully implemented, the layers grown are thick enough that LL can use an etch back cleaning process to improve the starting surface for their regrowth and totally resolve both the morphology and emitter resistance issues. A schematic for the HBT RTD integration is shown in Fig. 4, and a cross section in Fig 5.

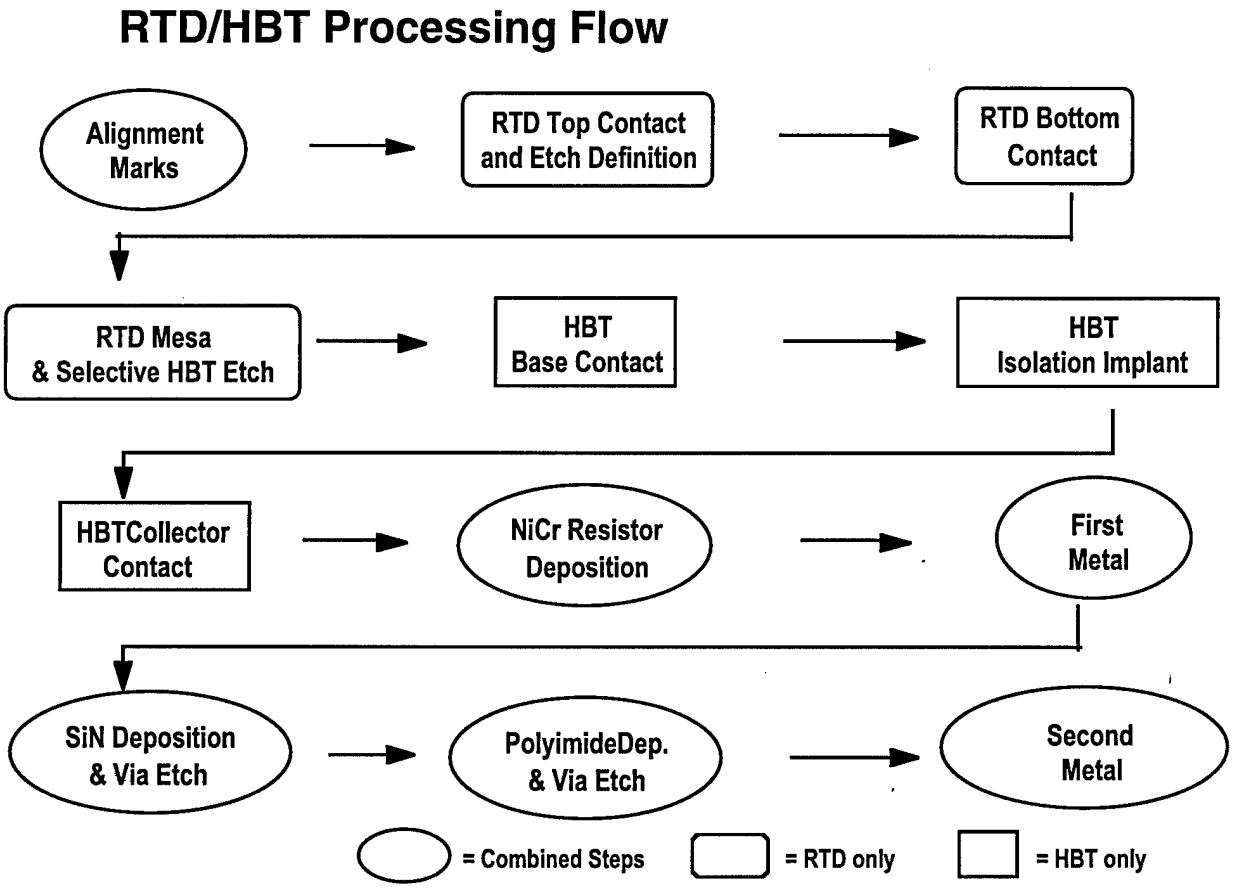


Fig. 4 Flow diagram of HBT/RTD process.

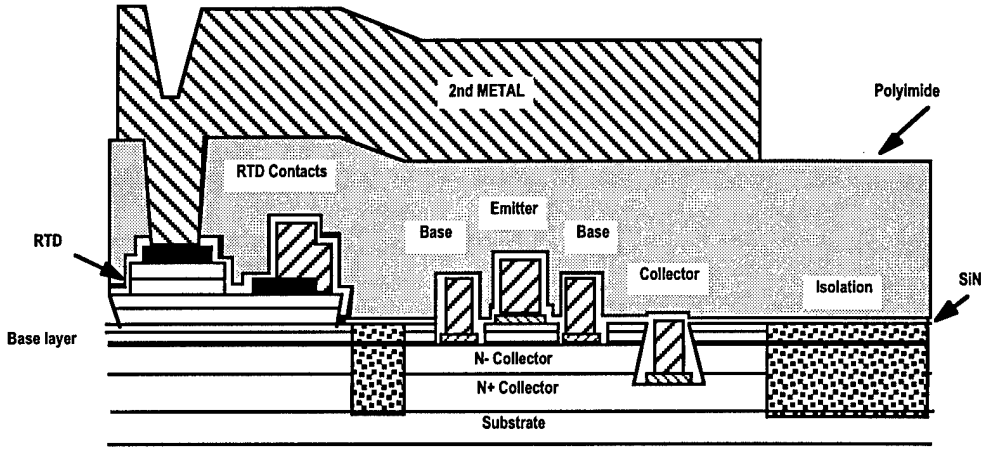


Fig. 5 HBT/RTD cross-section.

3.3 HFET Development

The fabrication procedure for a RTD/HEMT integrated circuits is illustrated in Fig. 6. Many of these procedures are the result of the development of our HEMT IC process and diode/HEMT process, which are reliable and high yield processes for GaAs LSI and MMICs. The process starts with MBE growth. As the first step, top RTD anode ohmic contacts of AuGe/Ni/Au (1200Å/300Å/800Å) are deposited with a presurface clean of diluted 5% HF dip, and the metal is lifted. The second step is to etch into the RTD cathode (bottom) contact layer using H_3PO_4:H_2O_2:H_2O = 10:10:200 etchant. Careful layout design and etching must be exercised to avoid undercutting the RTD or peeling the anode metal. The ohmic contact metal for the cathode layer is the same as anode. After anode and cathode metal contacts are made, the RTD mesa layer was selectively etched away to reveal the HEMT layers. This was done by using a selective citric acid:H_2O:H_2O_2 = 5mg: 500ml:100ml etchant to selectively remove InGaAs layer and stop at the thin AlAs layer above the HEMT layer. Overetching is necessary at this step to prevent the etching residuals from contaminating the surface. The thin AlAs stopping layer is then removed by using the 5% HF dip. The fabrication procedures HEMT followed the development of Rockwell's digital HEMT process. To maintain good planarity, device isolation was done by oxygen implantation. Because of the thermal stability of the oxygen implanted

region, the oxygen implantation was carried out before the ohmic contact alloying step. Following the isolation, the ohmic AuGe/Ni/Au was deposited for the HEMT ohmic contacts.

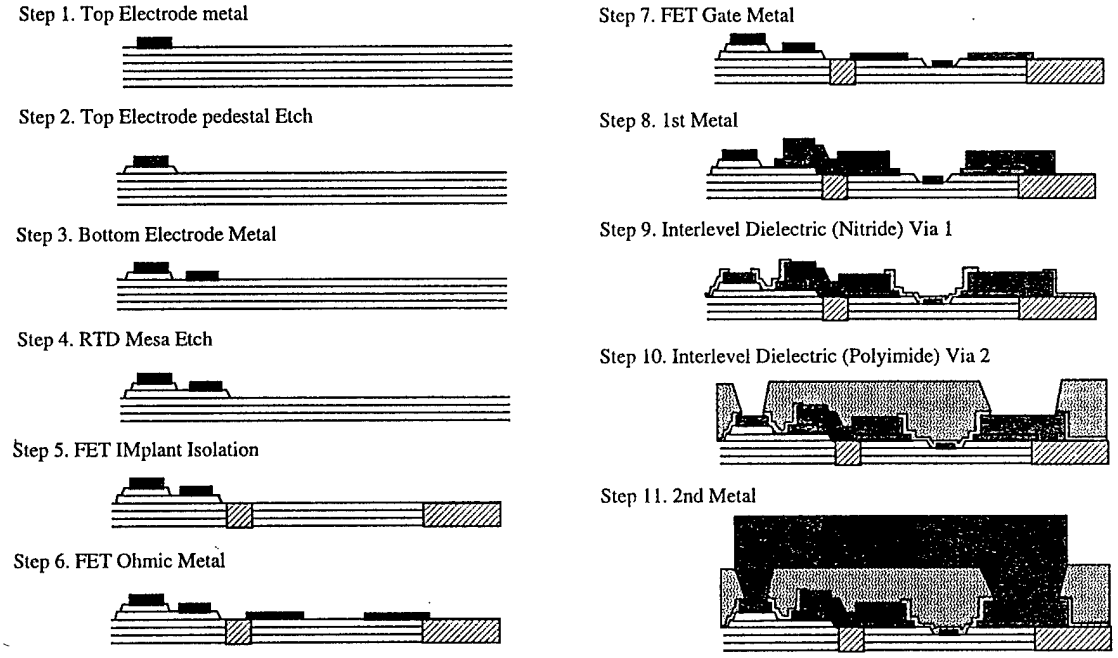


Fig. 6 RTD/HEMT process steps.

Two different Schottky metallization steps are used to fabricate enhancement mode devices and depletion mode devices. Reactive ion etching (RIE) is used to recess gates prior to Schottky metal evaporation. CCl_2F_2 + He plasma is used to selectively etch GaAs layers. For enhancement-mode devices, the etching stops at the surface of the GaAlAs layer and for depletion-mode devices, only the top GaAs layer is etched away. Because of the excellent etching selectivity, the threshold voltage variation due to gate recess is minimized. The threshold voltage control depends only on the MBE-grown layers, which are known to be very uniform. Typical threshold voltages for enhancement-mode devices and depletion-mode devices are 0.2 V and -0.6

V, respectively. To fine-tune the threshold voltage, we etched the channel by monitoring the channel saturated current. The Schottky metal used is Ti/Pt/Au. Ti/Au of first metal was deposited to make first metal interconnect. The device is passivated by a layer of 2000Å Si_3N_4 deposited by a photon-enhanced CVD system, and the first via was formed by reactive ion etching. A layer of 1μm polyimide was also coated to make devices more planar, and second via was formed by using reactive ion etching. Ti/Au is deposited and lifted for the second metal interconnect.

In all the processing steps, photolithography is important. The mask aligner used in this laboratory is an i-line GCA 5X step and repeat aligner. This aligner has excellent resolution (< 0.65 μm) and alignment accuracy (0.25 μm @ 3σ). With the combination of GCA resolution and some resist patterning techniques, even submicron geometries can be easily achieved.

3.4 RTD Etchback

Our original intention was that the overall thickness of the RTD layers would be <7000Å. This consideration is based on the photolithographic tools used and on the general notion of keeping the structure as planar as possible to increase the possible integration density. Since the simulation and layout of the circuits was started well before any actual wafers were fabricated, our decision was to use 3x3 μm^2 RTDs as the baseline RTD (for lower power consumption, smaller device size is desired). However, the final structure was actually over 1.5 μm (with buffer layers). This actuality required we reassess our proposed method for defining the RTD mesa, since it makes it very difficult to yield 3x3 RTDs. The original estimate of 7000Å would have made the topography no worse than the standard HBT collector. With the thicker layer, the need for more precise etching was obvious. For this process, we developed a methodology to dry etch the InGaAs and AlAs layers with little undercutting. The standard methods for this etch use an extremely high power reactive ion etch and a metal mask. The requirements of our HBT process include the need to lift off an SiN layer that passivates the RTD sidewall. We developed an RTD

etch in a Plasma-Therm ECR etching system that allows us to etch the RTD layers using a photoresist mask. We used a $CH_4/Ar/H_2$ plasma with the bottom electrode set at 200 V and the ECR source at 170 V. The bulk of the development effort was spent trying to optimize the ratio of CH_4 to the AR and H_2 to minimize polymer redeposition. The final etch condition was 2.5sccm CH_4/17sccm H_2/8sccm Ar. This etch still attacks the photoresist at about a 2:1 ratio to the InGaAs etch rate, which complicates monitoring the etch. The next step was to find selective etch stops on the HBT surface. For this, a thin 100Å AlAs etch-stop layer was added above the GaAs. A second GaAs layer was grown on top of the AlAs etch stop layer for good nucleation of the LTG buffer layer. Citric acid was used to etch through the InGaAs and GaAs layers that were left after the ECR etching and stopped on the AlAs. The AlAs and GaAs regrowth layer was then removed with a nonselective $H_3PO_4/H_2O_2/H_2O$ etch. The depth of this etch was determined by a combination of probing the surface until a breakdown of about 3V was seen, and surface profiling. Although this process was successful and we were able to demonstrate the first InGaAs/AlAs RTD with a GaAs HBT, further modifications were required to improve yield, by reducing the etch depth requirements. To the initial GaAs, regrowth was doped in the 10^{19} cm^{-3} range. This allows the formation of an acceptable emitter contact even if the etch does not completely remove the regrowth area. Unfortunately, we were unable to completely develop this process before the end of the contract.

3.5 RTD Process

The RTD we used for this contract is very similar to that developed by LL. The initial process uses a pseudorefactory metal contact to be used for the top RTD contact. The bottom contact is an alloyed contact with RTD isolation accomplished by using an etch that also exposes the HBT region. The first attempt at this process used the RTD top metal contact as an etch mask when etching down to the bottom contact. This was ultimately abandoned when the undercutting of this layer was greater than expected. Using an image reversal photoresist process, the same mask serves as the top contact mask and as the RTD mesa mask. Without the metal

mask, the undercutting was reduced significantly, but, as with all wet etching, there was still a small amount of undercutting. This made realignment of the top contact very difficult and resulted in the quantum well being shorted on some wafers. We then used the dry etching processing that had been developed for the RTD isolation process (explained in the HBT section) to form this mesa. This process solved the undercut issue, although at the end of the contract we were still investigating the effects of possible redeposition on the quantum well sidewalls. More work is needed to refine this process and define the proper c-factors (changing the pattern size on the mask to compensate for processing deltas).

3.6 Metal Interconnects

We actually expected more issues in this area than we encountered. The designs called for the same interconnect level (M1) to make contact to the HBT collector as well as the bottom RTD contact, a step of >2.0μm. We were concerned that with the depth of field on our 5x GCA aligner, that resolving lines over this height range would be problematic. (The Censor aligner we started the program with ran into this problem, and we subsequently changed over to the GCA to alleviate some of the alignment and depth of field issues). Initially, a process was developed that split the M1 into two masks, the first being exposed using the standard process and making contact to the HBT electrodes. The second mask is then exposed (in the same photoresist) with a focus offset to make contact to the RTD electrodes. Due to the sparse layout used in this program, this method was not required, but it will become necessary as the metal line width is reduced and circuit density is increased to LSI levels. Another area of concern is the ability of the metal to make the step heights required. To insure the best possible step coverage, we deposited metal in an e-beam evaporator with the wafers in a horizontal position. The wafers are then rotated around their centers, as well as globally, to insure uniformity. This system uses the angle of the plume as the metal is being evaporated to equal about a 30 degree angle of evaporation to cover the steps. A critical issue for this program was etching of intermetal vias. The second level metal interconnect (M2) was used to make contact to the top of the RTD. The via through the

polyimide was etched along with the standard metal 2 to first level interconnect (M1) vias. The issue here is that the polyimide used at the Science Center only planarizes about 60% (depending on step height as well as pattern size). This results in the polyimide over the top contact being significantly thinner than in the field area where the M2 to M1 vias are formed. This results in a significant over etch of the RTD via even when minimum etching was used to open the M1 to M2 via. The via overetch combined with mask misalignment led to a yield loss, as the via was not contained on top of the RTD contact, and the M2 was able to short the RTD sidewall. We will develop a process that uses a planarization layer and etch back between the polyimide coatings to keep the polyimide thickness uniform over steps. Although a separate via would also prevent this problem, the planarization process would also allow for additional interconnect metal layers to be used to increase circuit complexity, with about the same amount of process complexity.

3.7 Processing Summary

A process that allows for the fabrication of InGaAs/AlAs RTDs with GaAs HBTs and GaAs HEMTs has been developed and demonstrated. Key issues related to the device co-integration have been successfully addressed. To increase yield to the point of fabricating useful circuits, several key areas of the process need to be refined. These areas include: reducing the thickness of the buffer layer to decrease the topography, refining the photomask c-factors for proper device sizing, and developing a planarized interconnect process to increase circuit complexity and yield. Another important point is that with the exception of the CH_4 etching, all the components of this process are in place in Rockwell's production facility in Newbury Park, CA.

4.0 Device Design and Development

Several device and process related issues were addressed before layout and simulation could begin. The original baseline HBT was 1.4x3 μm^2 emitter planar (using an implant to define base). This makes the overall process more planar (improving yield) and reduces complexity, yet

provides enough current gain at low voltage bias to be useful for RAMs. There is a slight decrease in performance for the planar device compared to a mesa isolated device due to increase base-collector capacitance. Large value resistors were fabricated using the HBT base layer (300 Ω^2) rather than nichrome to decrease layout area. These devices are operated at 1-2 mA collector current. As such, we need to have an RTD that has a peak current that matches this bias current for the HBT. The HEMTs used for this program are similar to those used in SPICE models for these devices (HBT, RTD, and HEMT) were provided to the circuit designers. The HBT/RTD circuits were designed first, based on HBT models provided by Rockwell and RTD models provided by Lincoln Laboratory. The HEMT model was also provided to the designers. All of the RTD models were developed based on a PVCR of 9 and a peak voltage of 1 volt.

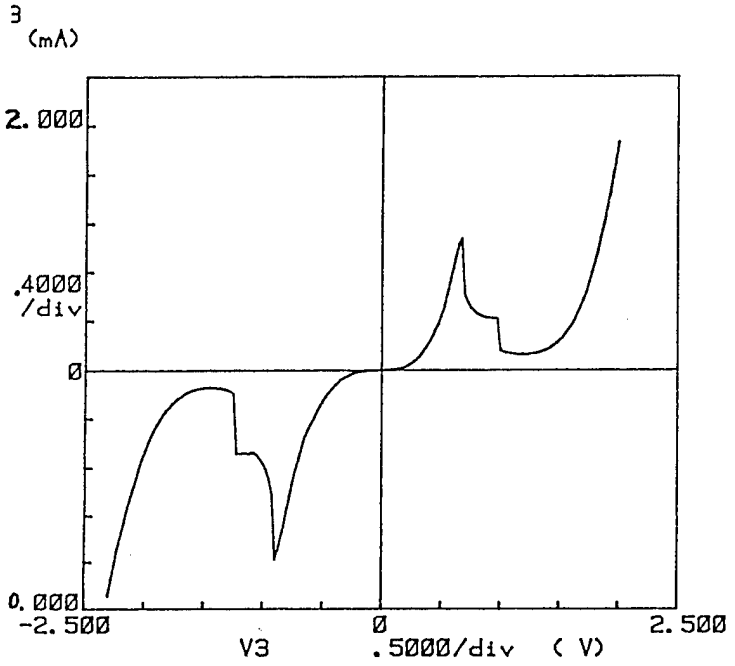
The "baseline" RTD for this program was a 9 μm^2 device with a peak current density of $2.0x10^4$ A/cm^2 ($I_{peak} \sim 2$ mA for the baseline device). This decision was based on the trade-off between manufacturability and low power. The RTD is contacted on the top mesa with interconnect metal 2, and on the bottom contact with interconnect metal 1. This allows it to be more synergistic with our existing metalization process. In addition, the use of emitter or FET ohmic as the bottom contact was investigated. The test results indicate that the FET ohmic can be used as the bottom contact, with no adverse effects. A novel single quantum barrier device is essentially free in the process by using a FET ohmic level to RTD bottom contact (the AlAs etch-stop acts as a single barrier varactor).

Mask layer definitions and design rules were decided on for this program. The HBTs/HEMTs and RTDs were intentionally kept as separate devices. This allows the conventional transistors and the RTDs to be connected in any orientation. In addition, the limit of a 3x3 RTD makes direct integration on the HBT emitter undesirable. The mask layers refer to the layer identification in the CAD tools used to lay out the circuits (shown in Table 1).

Table 1

Mask Layers for HBT/RTD Mask		
2	IS	isolation
3	EM	light field emitter
5	BC	base contact metal
6	DR	dielectric removal layer
7	CC	collector contact
8	RES	nichrome resistor layer, 50 ohm/square
9	M1	level 1 interconnect metal-metal 1
10	SINV	silicon nitride via- 1st dielectric between m1 and m2
11	M2	level 2 interconnect metal-metal 2
16	MIMV	nitride via- used to define mim capacitors
23	DEM	dark field emitter (defines contact to emitter)
31	MESA	mesa definition for rtd
32	RVIA	via contact to rtd
33	RM1	top contact to rtd
34	RM2	bottom contact to rtd
40	PISO	base layer for planar process
TOTAL	16	
Mask Layers for HEMT/RTD Mask Set		
2	IS	isolation
8	RES	nichrome resistor layer, 50 ohm/square
9	M1	level 1 interconnect metal-metal 1
10	SINV	silicon nitride via- 1st dielectric between m1 and m2
11	M2	level 2 interconnect metal-metal 2
16	MIMV	nitride via- used to define mim capacitors
31	MESA	mesa definition for rtd
32	RVIA	via contact to rtd
33	RM1	top contact to rtd
34	RM2	bottom contact to rtd
41	SAIN	saint layer for HEMT/MESFET gate
54	OHM	ohmic contact layer for FETs
55	DGT	d-gate for FETs
56	EGT	e-gate for FETs
TOTAL	15	

RTDs have been fabricated in the pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs material system on GaAs substrates that have peak-to-valley current ratios (PVCRs) of approximately 9 and peak voltages of approximately 1 V at room temperature. The IV anneal for this device is shown in Fig. 7 for devices at LL and in Fig. 8 for those fabricated at Rockwell. The structure for these devices was originally developed on (100) substrates, and subsequently demonstrated on (100) 2 degrees off toward (110) (on commercially available MOCVD HBT epilayers). Surface preparation was critically important to obtain the high PVCRs demonstrated here. The PVCRs demonstrated are 50% better than any reported RTD using the lattice-matched AlGaAs/GaAs or AlAs/GaAs material systems on GaAs substrates.



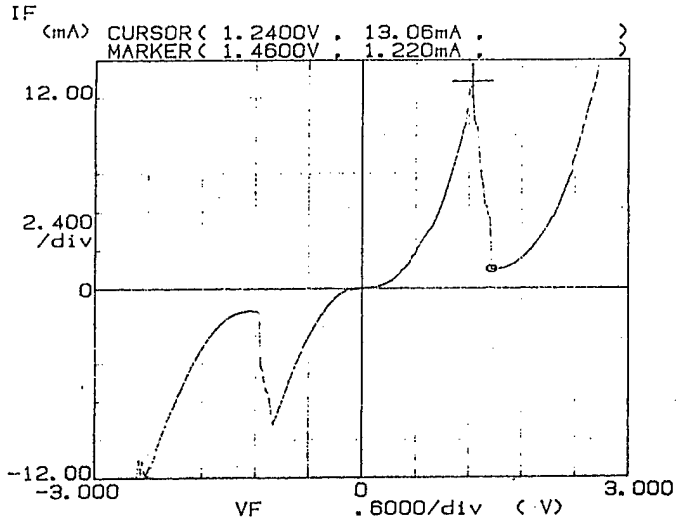
Forward:
I_p = 1.07 mA @ .675V
I_v = 127.9 µA @ 1.175V

I_p/I_v = 8.4

Reverse:
I_p = 1.574 mA @ 0.9 V
I_v = 144.5 µA @ 1.45 V

I_p/I_v = 10.9

Fig. 7 I-V characteristics of RTD fabricated at LL, using same wafer as Fig. 8.



Forward:
I_p = 13.06 mA @ 1.24V
I_v = 1.20 mA @ 1.48V

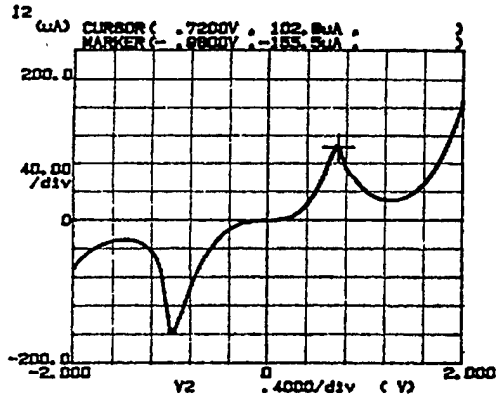
I_p/I_v = 10.9

Reverse:
I_p = 8.63 @ 1V
I_v = 1.43 @ 1.3 V

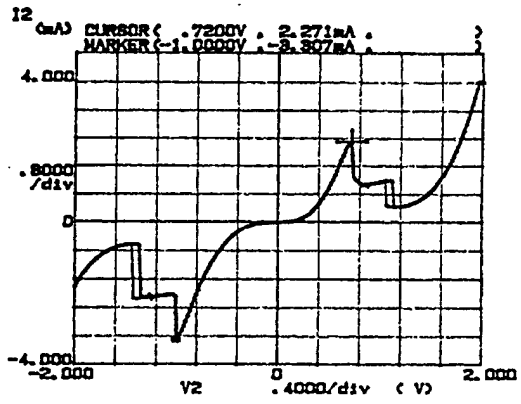
I_p/I_v = 6.0

Fig. 8 I-V characteristics of RTD fabricated at Rockwell, using material provided by Lincoln Laboratories.

Using RTDs fabricated in the above material system, with PVCR=5 (due to surface preparation difficulties), at Rockwell Science Center we have demonstrated RTDs with ON MASK dimensions of 1.5x1.5, 2.0x2.0, 1.4x3.0, 5.0x5.0, and 3x1.4x8.5 μm^2. The I-V curves for these devices are shown in Figs. 9 and 10. The peak position of these RTDs in less than 1 volt, and is relatively insensitive to device size. Because of the extreme undercutting of a wet chemical etch, the 1.5 square RTD is most likely a submicron device. Large area HBTs have been fabricated on the same wafer as the RTDs discussed above. Gummel plots for these HBTs are shown in Fig. 11. This represents the first time that lattice mismatched RTDs and HBTs have been demonstrated on the same wafer. The process flow is the same as in (A), and the schematic for the process used to fabricate these devices is shown in Fig. 12.

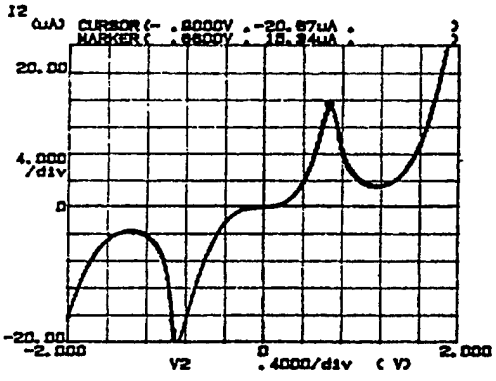


2x2 mm^2 RTD



5x5 mm^2 RTD

1.5x1.5 mm^2 RTD



1.4x3 mm^2 RTD

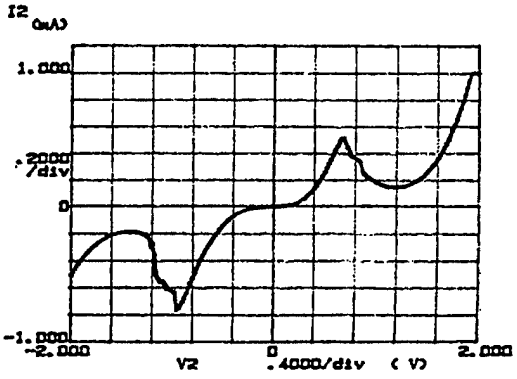


Fig. 9 RTD (on HBT) IV curves for different devices.

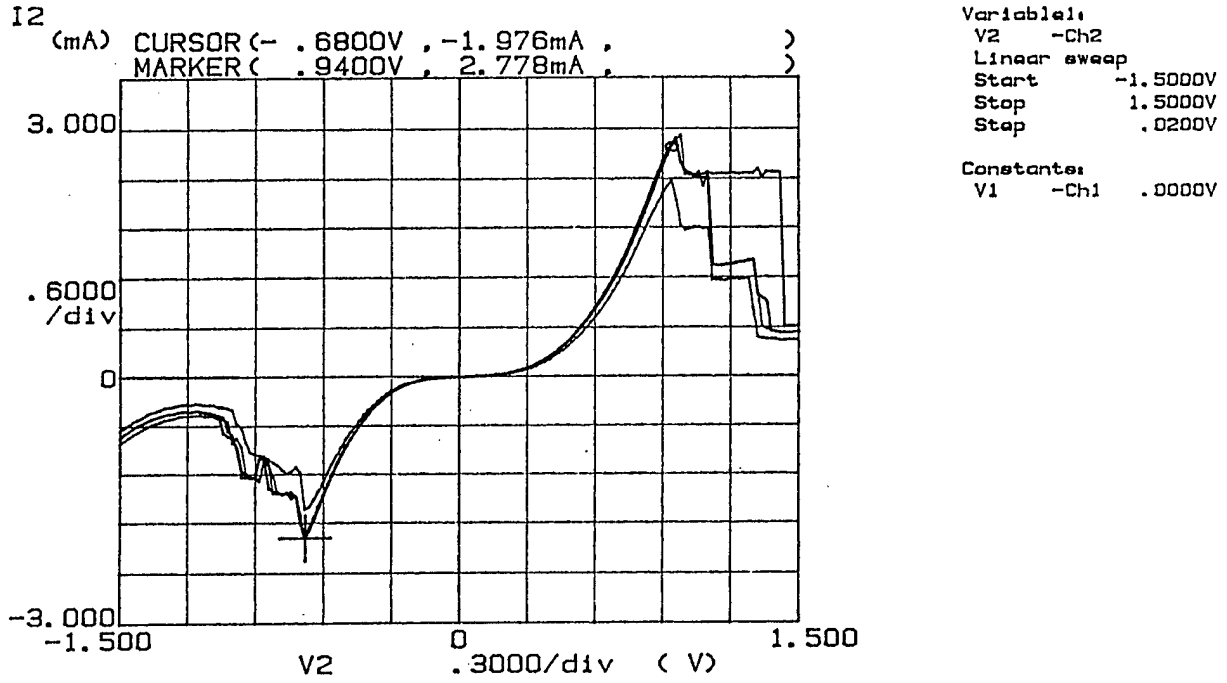


Fig. 10 IV curve for 3 X 1.4 X 8.5 μm^2 RTDs on same wafer as devices from Fig. 9.

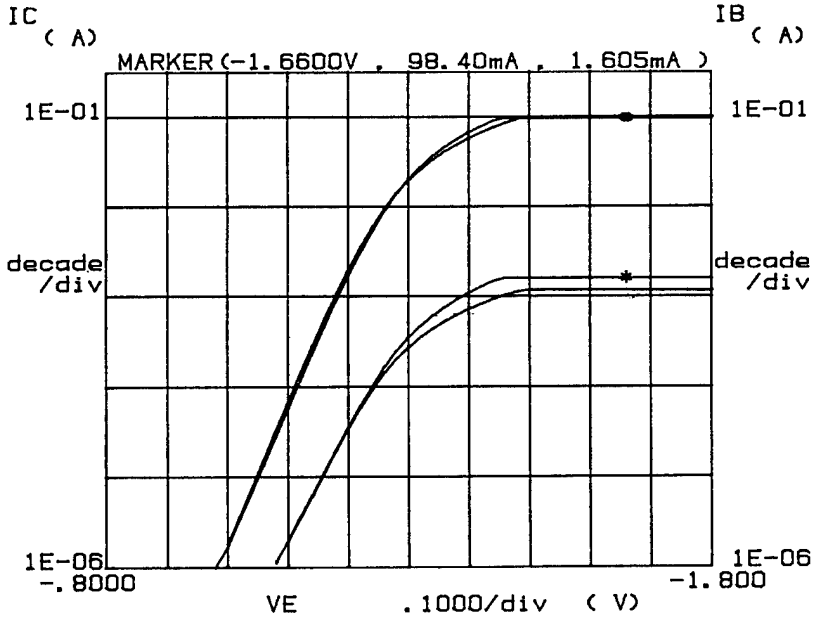


Fig. 11 Gummel Plot of 67 X 67 μm^2 HBTs on the same wafer as RTDs.

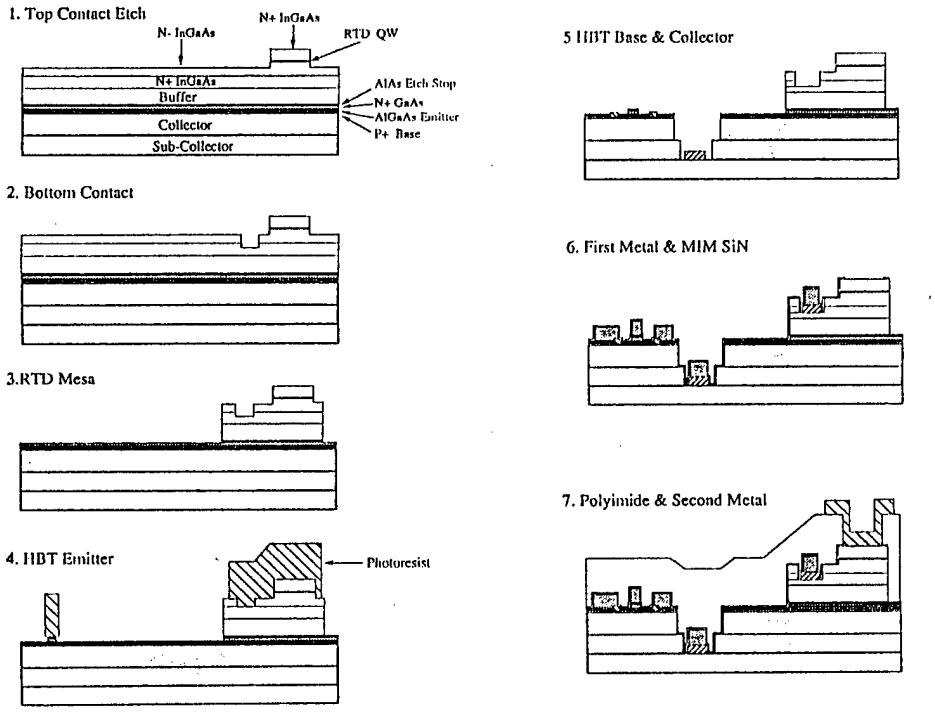


Fig. 12 Process schematic (not to scale) for HBT/RTD co-integration.

A lot of 2 wafers was processed to evaluate the current process for this integration, before committing a full lot. We demonstrated that both small area HBTs (1.4x3 μm^2 emitter) and RTDs (4x4 μm^2) can be fabricated, even though the material system for the RTDs is heavily lattice mismatched to the HBT epitaxial layers. The IV curves for the two devices is shown in Fig. 13. This is the first time that lattice mismatched RTDs and HBTs have been cointegrated on the same wafer. Testing of metal step coverage patterns had good yield, indicating that the topology of the wafer should not present any significant yield problems. Our testing also indicated that the following changes in our processing would be needed to improve device yield: 1) dry etch the RTD mesa to prevent metal shorting to RTD sidewall, 2) passivate the sidewall earlier in the process, 3) modify the MOCVD (HBT) structure to lower the emitter contact resistance, and 4) modify the MBE structure to include a contact layer for the HBT emitter.

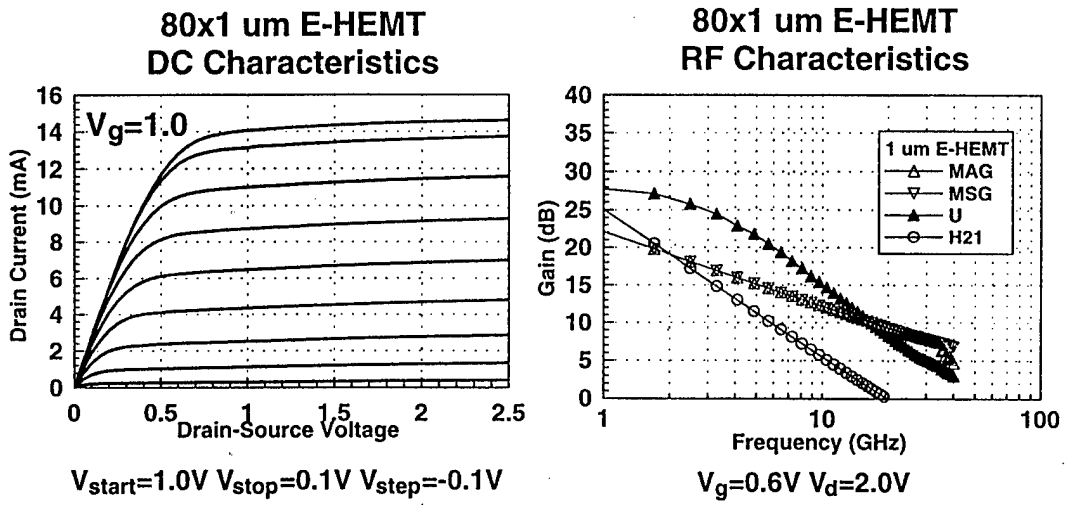


Fig. 13 DC and RF characteristics of HEMT after removal of lattice mismatched RTDs.

To lower the HBT emitter resistance (which has a significant impact on RF and analog performance), the RTD to HBT buffer layer will be doped. In addition to the doping, the indium concentration will be graded. These two modifications have two effects: lower the emitter contact resistance and relax the tolerance of the etch used to uncover the HBT emitter.

AlGaAs/GaAs RTDs on HEMT peak to valley current ratio was excellent (3.4). However, the peak voltage was high, probably due to contact resistance. A typical RTD IV curve is shown in Fig. 14.

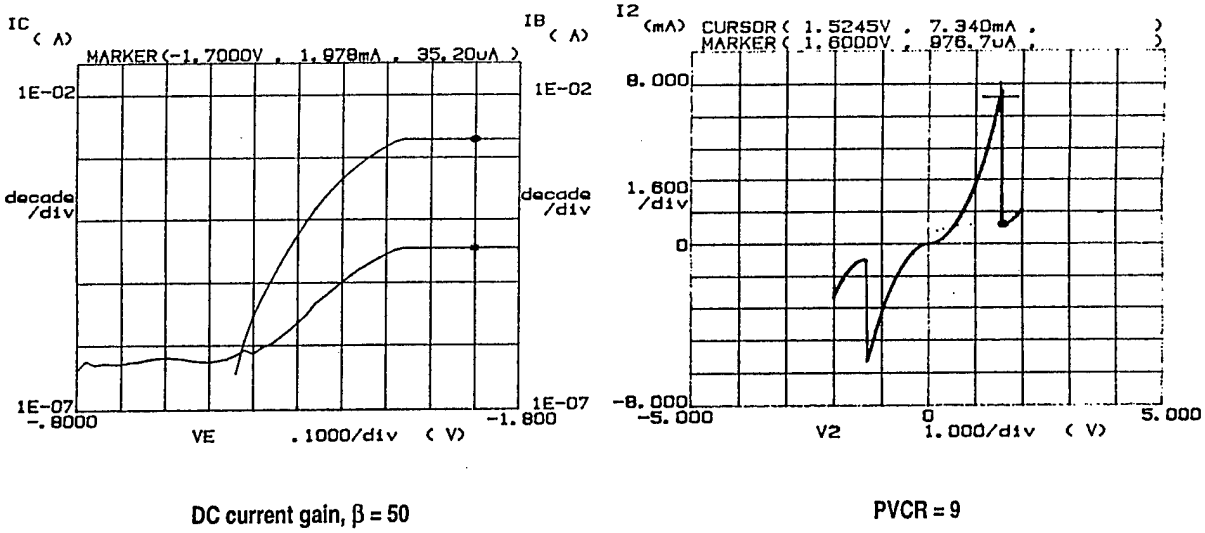


Fig. 14 IV curves of HBT and lattice mismatched RTD in same wafer field.

The Science Center's AlGaAs/GaAs E-D HEMT process was determined to be adequate for many of the system applications that LL would like to target. This process is well-established and has demonstrated very high yield HEMT RAMs. This will allow LL to concentrate on developing InP-based HEMT. The HEMT DC and RF characteristics are shown in Fig. 15.

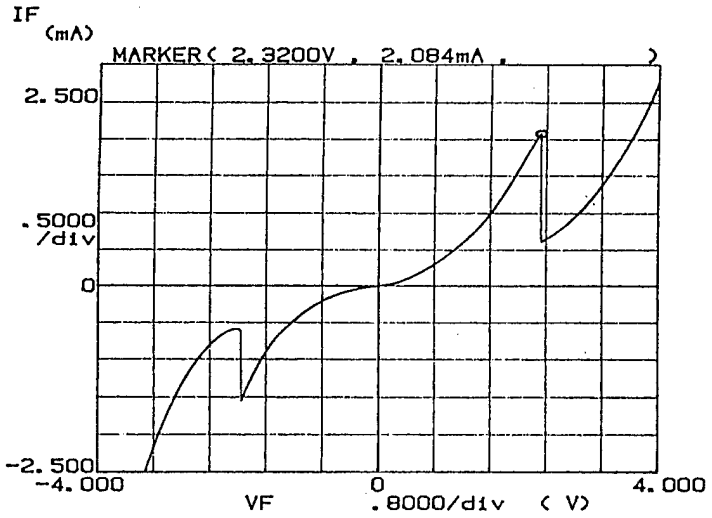


Fig. 15 AlGaAs/GaAs RTDs on HEMT (Peak to Valley ratio = 3.4).

5.0 Circuit Design, Simulation, and Testing

5.1 RTD/HBT Circuits

Several RTD/HBT circuit topologies were investigated. The first logic studies were the Resonant Current Injection Logic (RI^2L) family, where the RTD is used as a pull-up load (i.e., as a nonlinear load element), which allows the power dissipation to be decreased while maintaining high switching speed. This logic family requires current limiting resistors to limit the base current. Since these resistors are fairly large, the base layer (providing approximately 300-400 Ohms per square) was used instead of NiCr, which is 50 Ohms per square. Bypass capacitors are also required for these gates to charge the base-emitter junction at high speeds. The combination of the limiting resistor and the collector match the internal RC of the HBT. Since the nominal

capacitance is on the order of 0.05 pF, these are also fairly large. Ring oscillators were simulated in SPICE using this circuit topology. The RTD current sources provide an instantaneous surge of current to allow for fast switching. The simulation results for these ring oscillators indicate that gate delays of 47 ps (oscillation at 3.3 GHz for a 13 stage ring oscillator) can be achieved with a simulated power of 12mW. Prescalars, such as the one in Fig. 16, were also investigated using this logic family. Prescalars such as 128/129 Dividers are used in phase-locked loops and communication systems where high speed and low power are required. These circuits are simulated to use an average power of 57 mW at 1GHz input frequency. The simulation result is shown in Fig. 17.

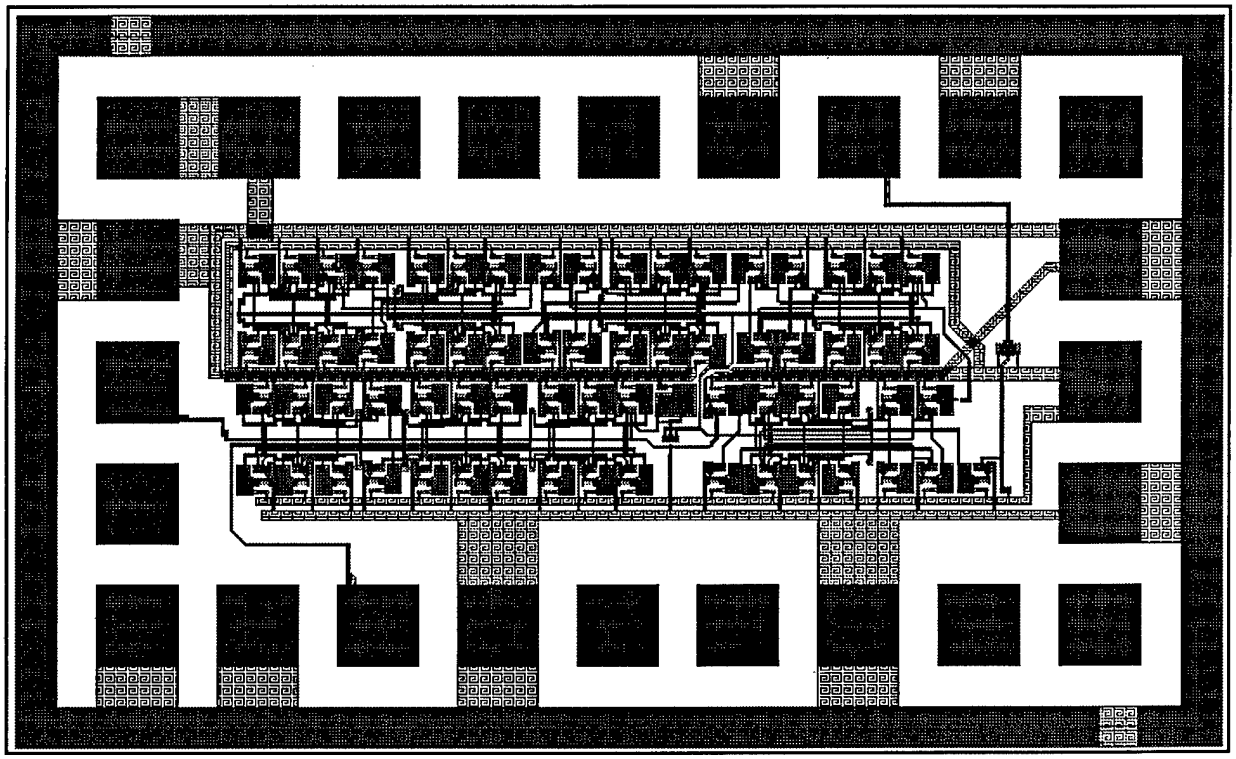


Fig. 16 Layout of 128/129 prescalar.

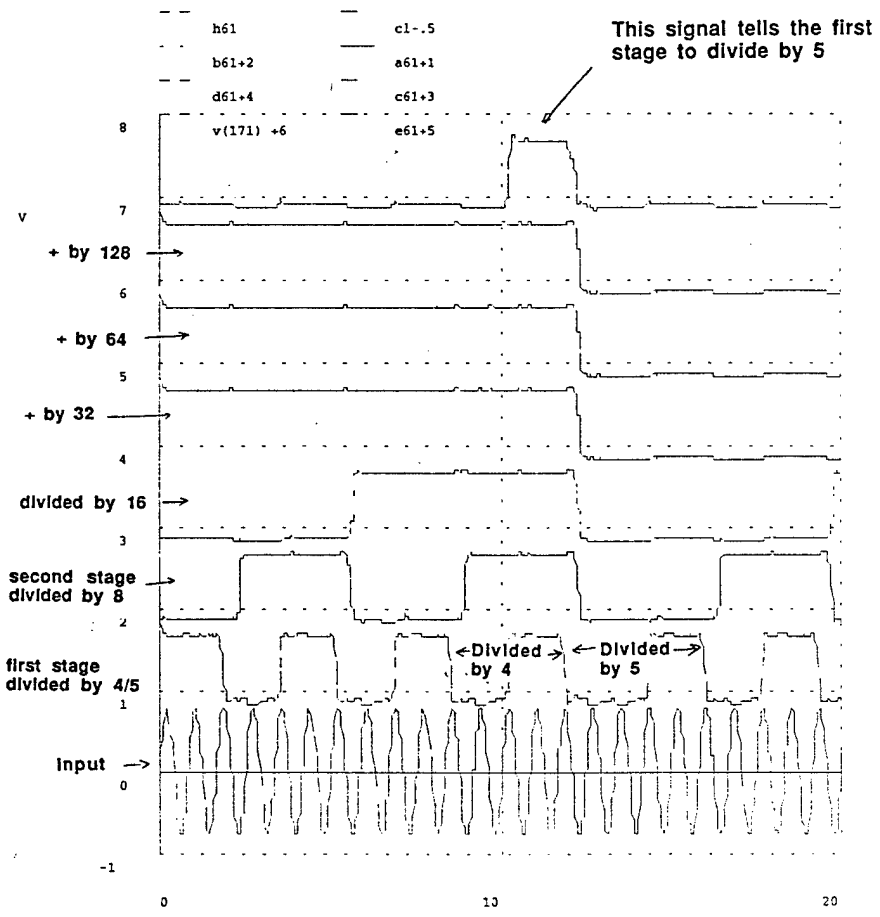


Fig. 17 Simulation results for 128/129 prescalar.

The second logic family we investigated is the Resonant Emitter HBT Logic (REHL) family. Since the RTD IV curve behaves as a basic logic function, it suggests the use of RTDs in basic logic gates. An XNOR gate can be based on a single RTD and 2 HBTs. This can greatly reduce the complexity and amount of area used for large logic circuits, resulting in lower power dissipation and higher functionality per chip. A variety of logic gates were simulated and laid out for this technology. A full adder using the architecture proposed by Takatsu et al. in the 1991 GaAs IC Symposium has been simulated. A schematic of this design is shown in Fig. 18. This adder uses an InGaAs RTD connected to the emitter of an HBT as the basic gate (REHBT logic). Two XNOR gates are used to perform the essential arithmetic operations, and a majority logic

gate is used to perform the carry operation. The layout is shown in Fig. 19. The biggest advantage of our approach is that the circuit will operate at room temperature and simulated to 1000 times the speed of their published results. Our simulation results are shown in Fig. 20. Other circuits such as multipliers, (Fig. 21) fan-out chains, and ring oscillators were simulated and laid out for this technology.

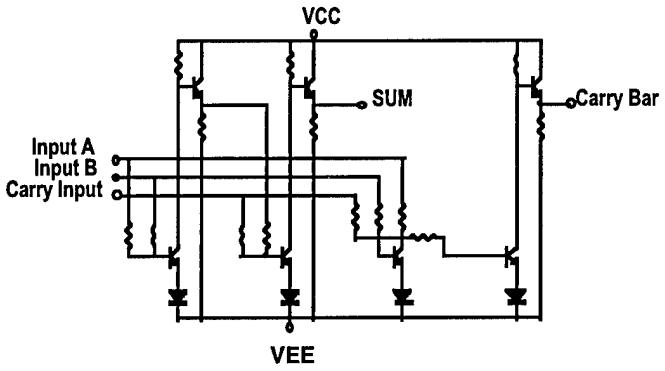


Fig. 18 Schematic of full adder circuit based on REHL logic.

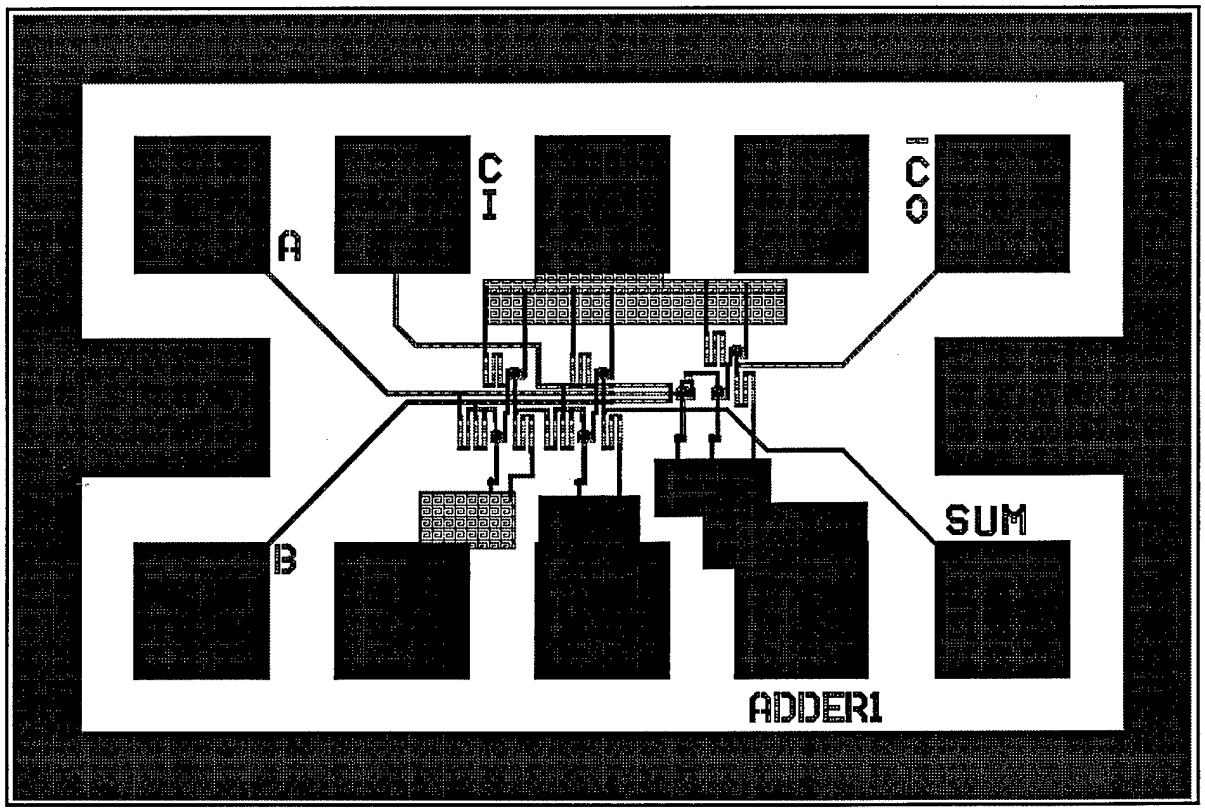


Fig. 19 Layout of full adder.

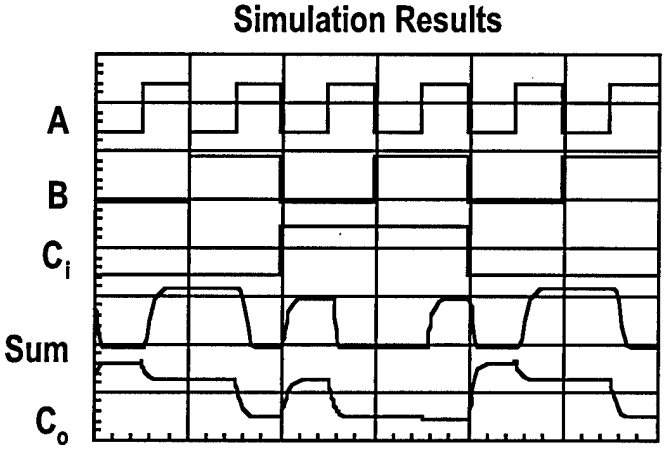


Fig. 20 Simulation results for full adder circuit.

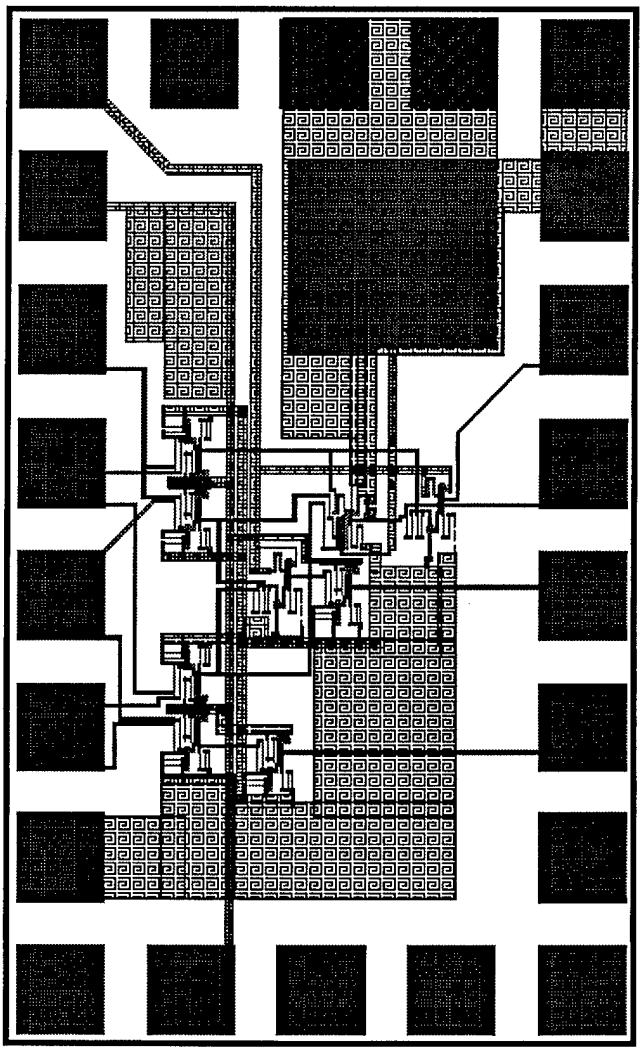


Fig. 21 Layout of 2 X 2 multiplier.

Finally, we studied RTDs integrated with HBTs for static RAM applications. Since RTD pairs are bistable, they can offer high density of integration to make more compact, lower power systems. Smaller RTDs can be used to reduce power consumption, and vertically integrated structures can offer further area reduction. With these goals in mind, a static RAM cell was designed and simulated. Rather than using 3 RTDs for the bit cell, an HBT was used to replace the readout diode. The bit cell and simulation results are shown in Figs. 22 and 23, respectively. The writing operation is shown in Fig. 24. A differential pair sense amplifier was also designed and simulated; the amplifier and its operation are shown in Fig. 25. A full HBT/RTD RAM based on this concept was also designed, and the layout is shown in Fig. 26.

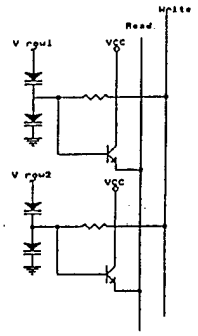


Fig. 22 RTD/HBT Bit Cell Schematic.

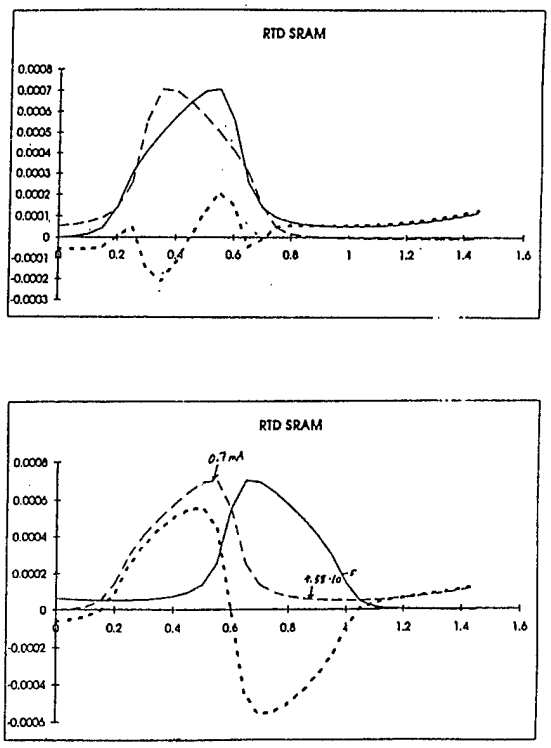


Fig. 23 Simulation of RTD/HBT Bit Cell.

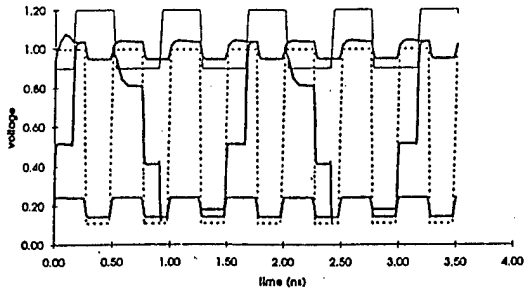
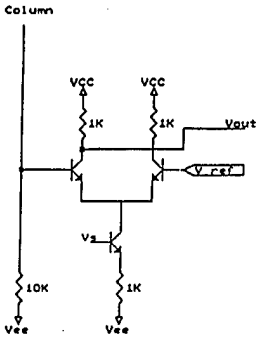


Fig. 24 Simulation of WRITE operation for RTD/HBT Bit Cell.

Read Operation:
• Vdd hold = 1.2V Vdd read = 1.5V

Sense Amplifier
• Vcc = 0V Vee = -4V



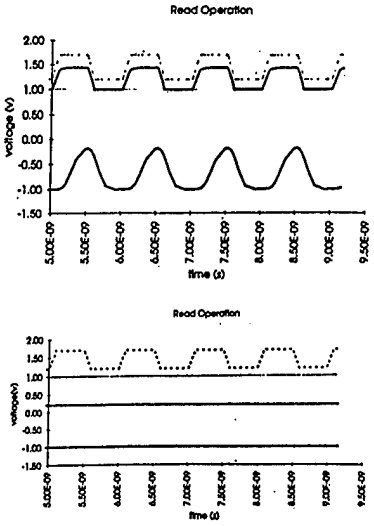


Fig. 25 Schematic and simulation of sense amplifier.

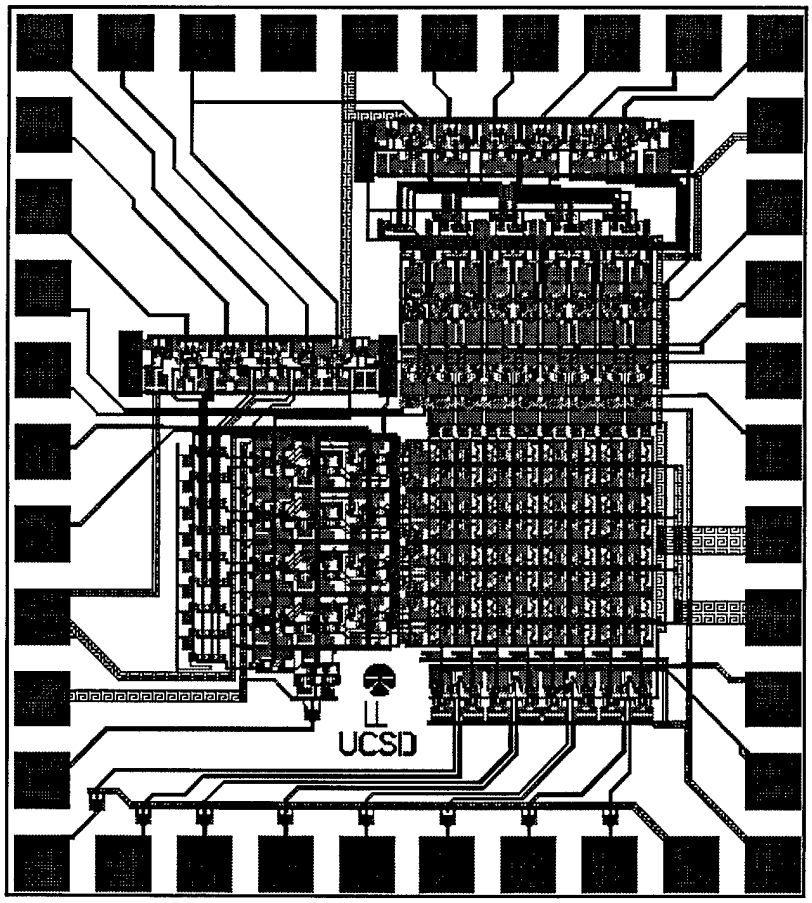


Fig. 26 Layout of 64 bit HBT/RTD static RAM.

Two dedicated HBT/RTD mask sets were fabricated. The floor plans for these masks are shown in Figs. 27 and 28.

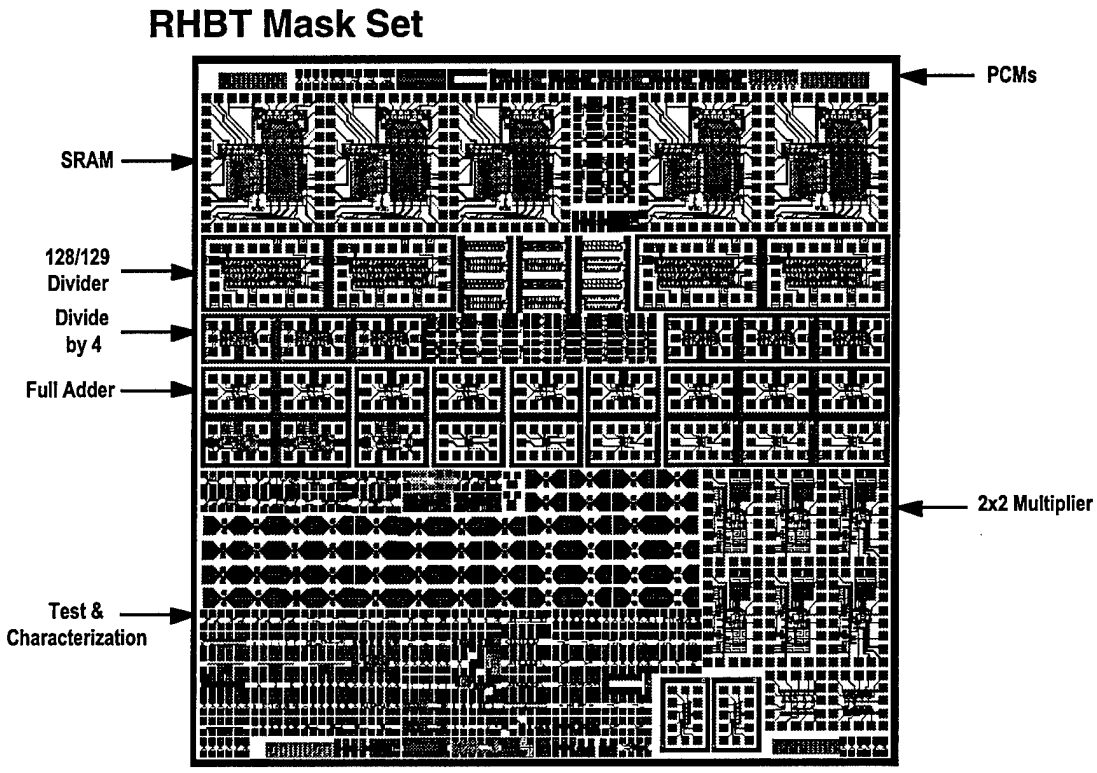


Fig. 27 RTD/HBT Mask Set.

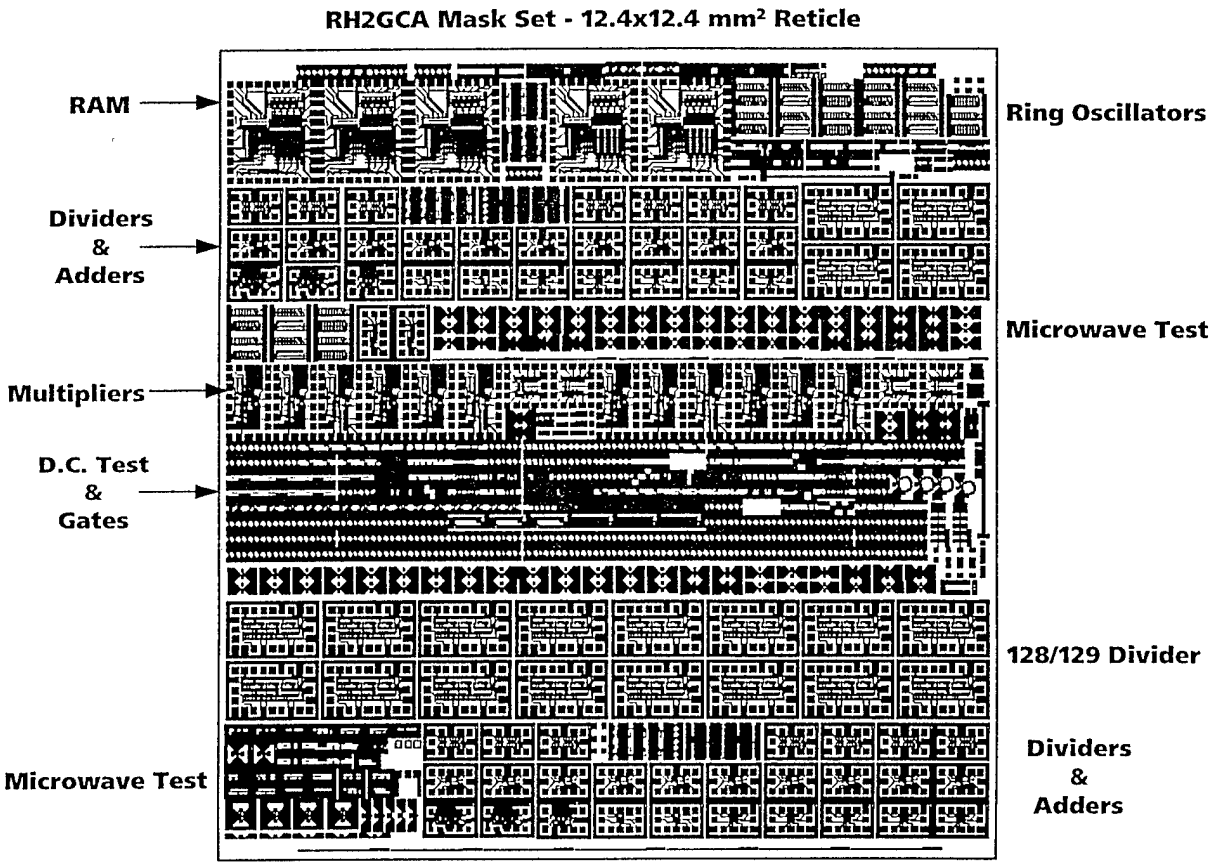


Fig. 28 RH2GCA Mask Set.

5.2 RTD/HFET Circuits

Direct RTD HEMT Logic (DRHL) Family

This family of logic is similar to Direct Coupled FET Logic (DCFL). The RTDs are used as loads instead of the standard resistor or depletion mode FETs. Similar to the description of RI_2L RTD/HBT integration, the peak current of the RTD serves as a boost current to increase the switching speed, while the valley current serves as static current in the low state, reducing the static current consumption. Basic gates and test circuits, such as inverters, NAND gates, NOR gates, fanout arrays, ring oscillators, and frequency dividers were designed and laidout for this logic family.

Basic buildingblocks for digital logic, such as inverters, NOR, and NAND gates were designed based on the LL RTD and the Rockwell E/D HEMT technology. Note that the particular architecture used for the NOR gate allows it to function as a latch if different input levels are used. Figure 29 shows the transfer curve for a DCFL gate with an RTD load. The hysteresis in the transfer curve is a result of the RTD. Several HEMT/RTD gates can be connected to form ring oscillators, such as the one shown in Fig. 30. These circuits provide information on both the device performance and manufacturing yield. The simulation results shown in Fig. 31 indicate a gate delay of 130 ps for a 19-stage ring oscillator, with a fanout of one. Frequency dividers are another circuit that is typically used to benchmark a technology. Such a circuit has been designed for this. The divider consists of two D Flip-Flops (made up of two- and three-input DCFL/RTD NOR gates) and some inverters. Simulation results of a divider operating at 1 GHz, along with a layout, are shown in Figs. 32 and 33. Finally, a HEMT/RTD shift register based on RTDs hold elements and HEMTs pass-gate elements was simulated and laidout. The schematic and layout of this chip are shown in Figs. 34 and 35, and simulated output in Fig 36. Some simple HEMT only circuits were included on the mask as process monitors and to provide a comparison to the HEMT/RTD circuits.

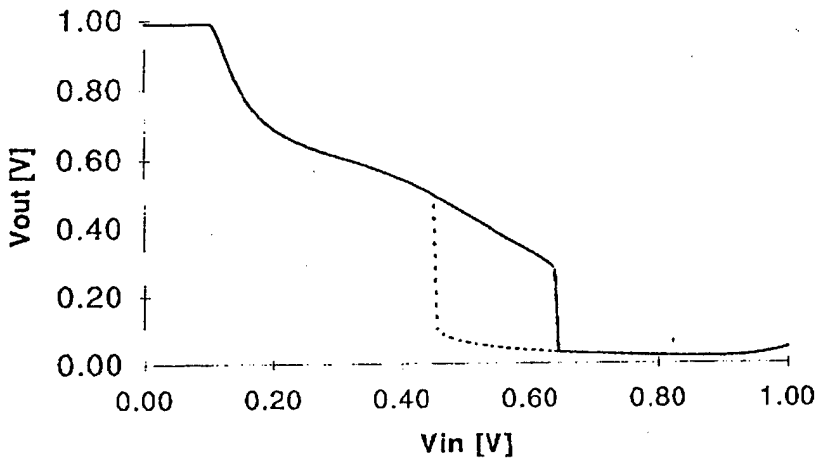


Fig. 29 DCFL with RTD load transfer curve.

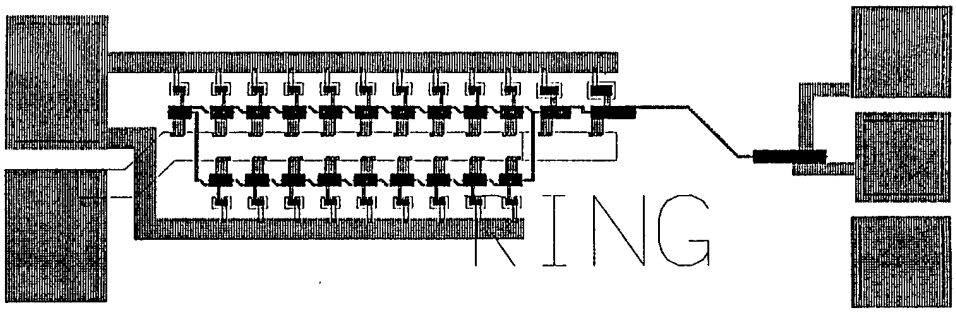


Fig. 30 19-Stage Ring Oscillator Layout.

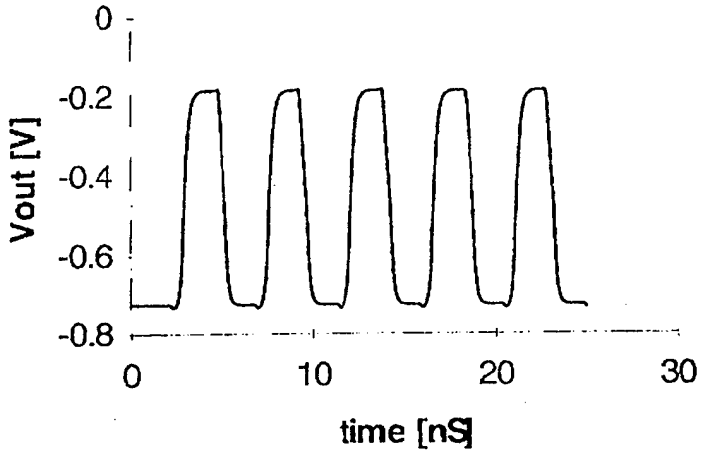


Fig. 31 Ring Oscillator simulation results. The gate delay is 130 ps.

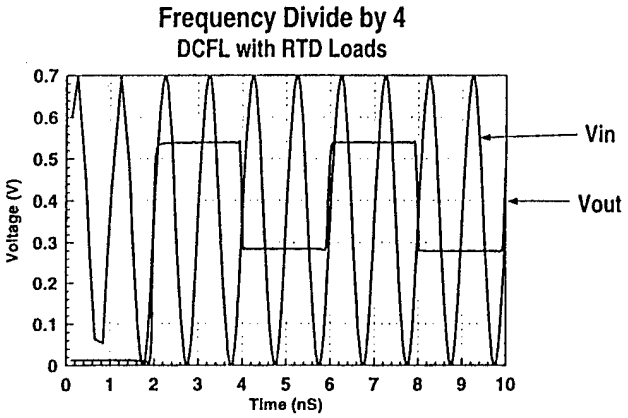


Fig. 32 Simulation of Frequency Divide by 4 using DCFL with RTD.

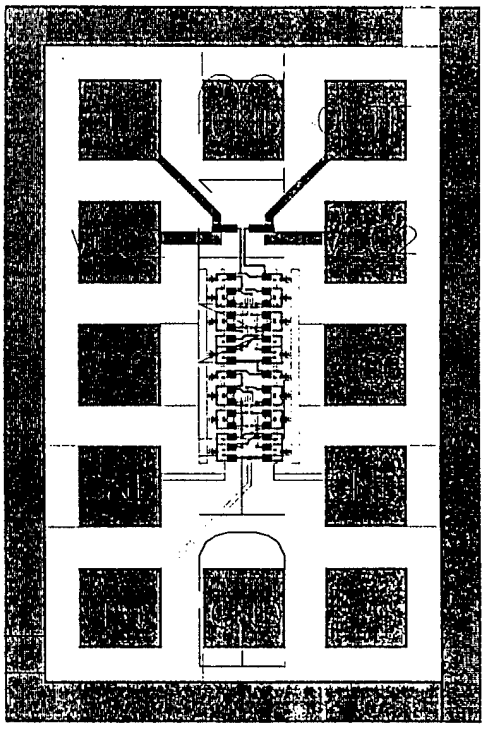


Fig. 33 Layout of Frequency Divide by 4.

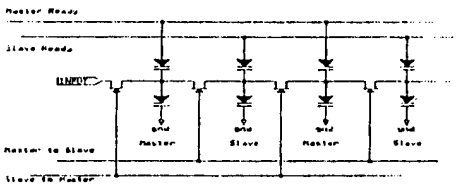


Fig. 34 RTD/HEMT Shift Register Schematic.

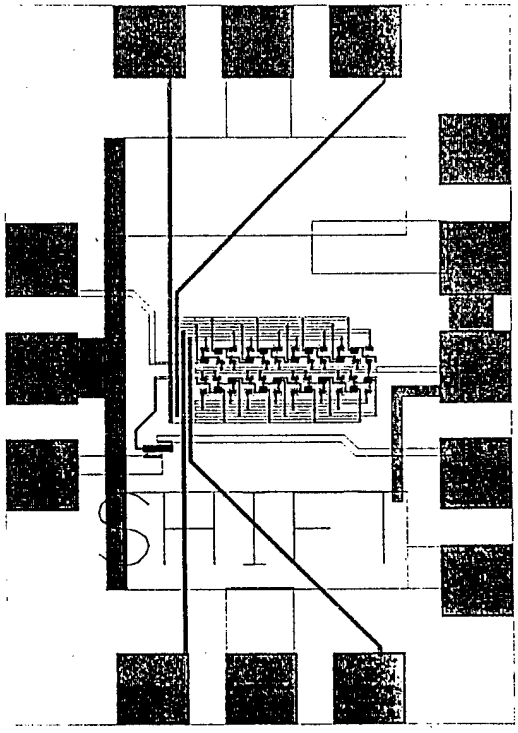


Fig. 35 RTD/HEMT Shift Register Layout.

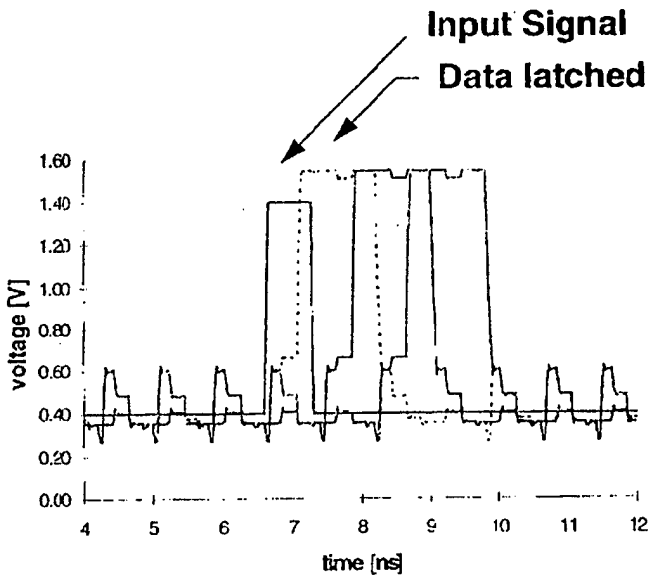


Fig. 36 Shift Register Simulation Results.

HEMT/RTD SRAM

Since an RTD pair can exhibit bistability, it can be used as the basis of a static memory cell. A detailed description of this bistability was presented earlier. For this circuit, the HEMTs were used as column drivers and I/O controls. Some small HEMT/RTD RAM concepts, such as the one shown in Fig 37, were designed and laidout. These include a single memory cell, shift registers, and 4x4 memory cell arrays.

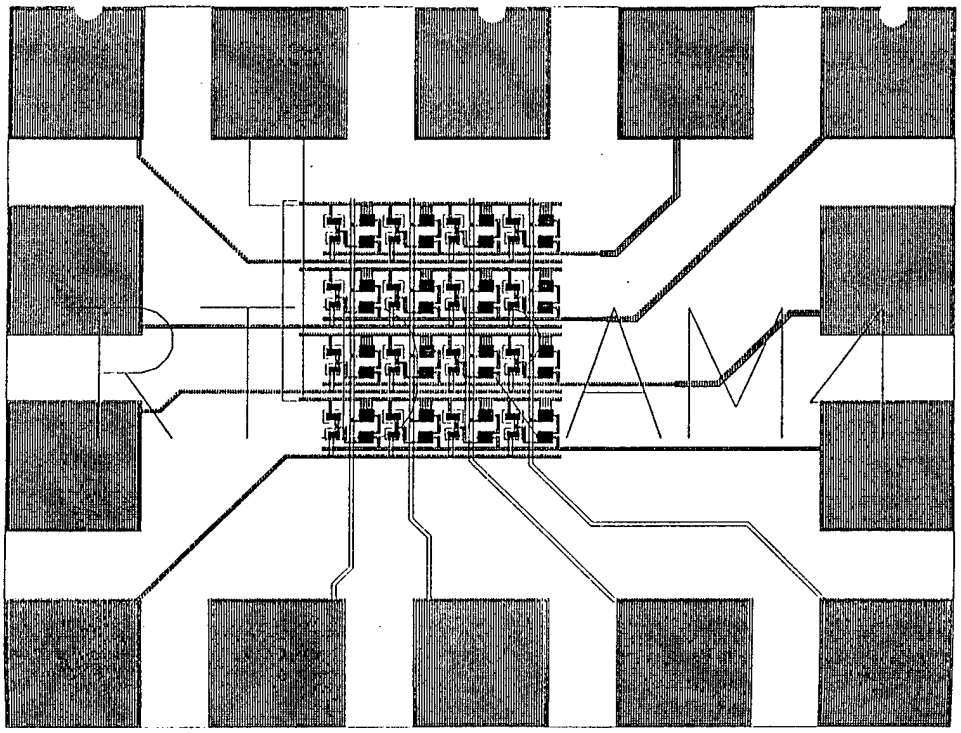


Fig. 37 Layout of RTD/HEMT RAM Concept.

In addition to the above circuits, a large number of modeling and process development structures were developed. Although the RTD is a very well-studied device from a physics standpoint, very little work has been done in characterizing these devices for circuit applications. Issues such as device scaling, uniformity, and reliability have received little attention. For RTDs to enter into the marketplace, issues such as these must be addressed. We have developed an extensive series of test patterns to investigate some of these issues. Other modeling and process test structures have been included to allow the HBTs and HEMTs on this program to be fully characterized as well.

A floorplan of the HEMT/RTD mask set are shown in Fig. 38. The contents of these masksare included in Appendix B.

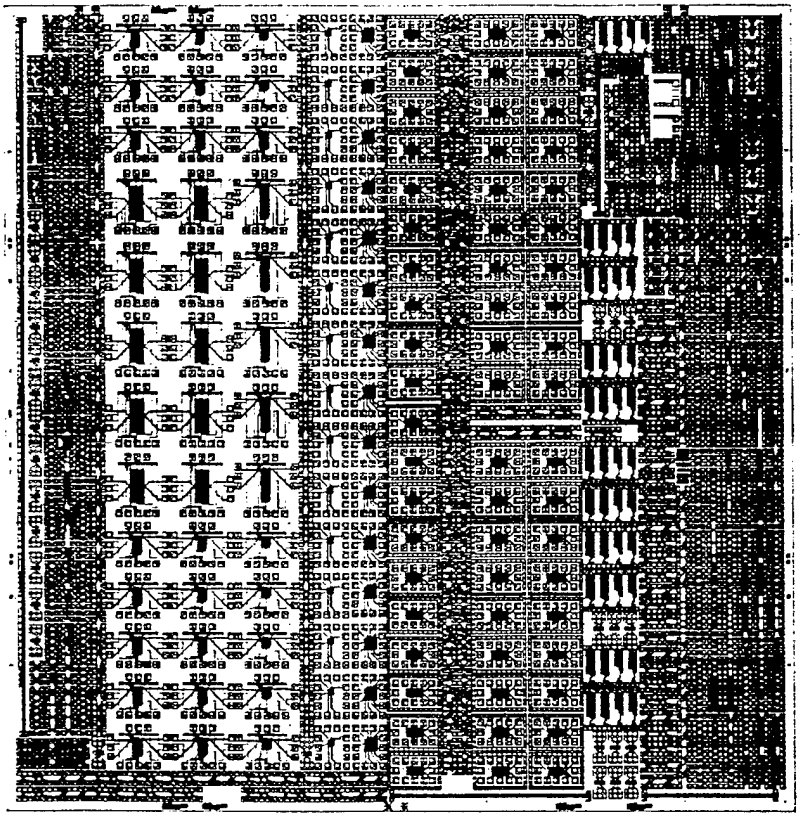


Fig. 38 HEMT/RTD mask set. Reticle is 12.7 mm x 12.7 mm.

RTD/HEMT Test Results

This section addresses the test results of the various wafers run in the HEMT/RTD technology. None of the RTDs fabricated on the HEMT material showed PVCR greater than 4. At present, it is not known whether this was due to the starting material or to processing related issues. Most of the processing for this portion of the program was done on quarters of 3" wafers, due to a limited material supply. One of the wafers had sufficient PVCR to enable the demonstration of basic logic gates, as shown in Figs. 39 and 40.

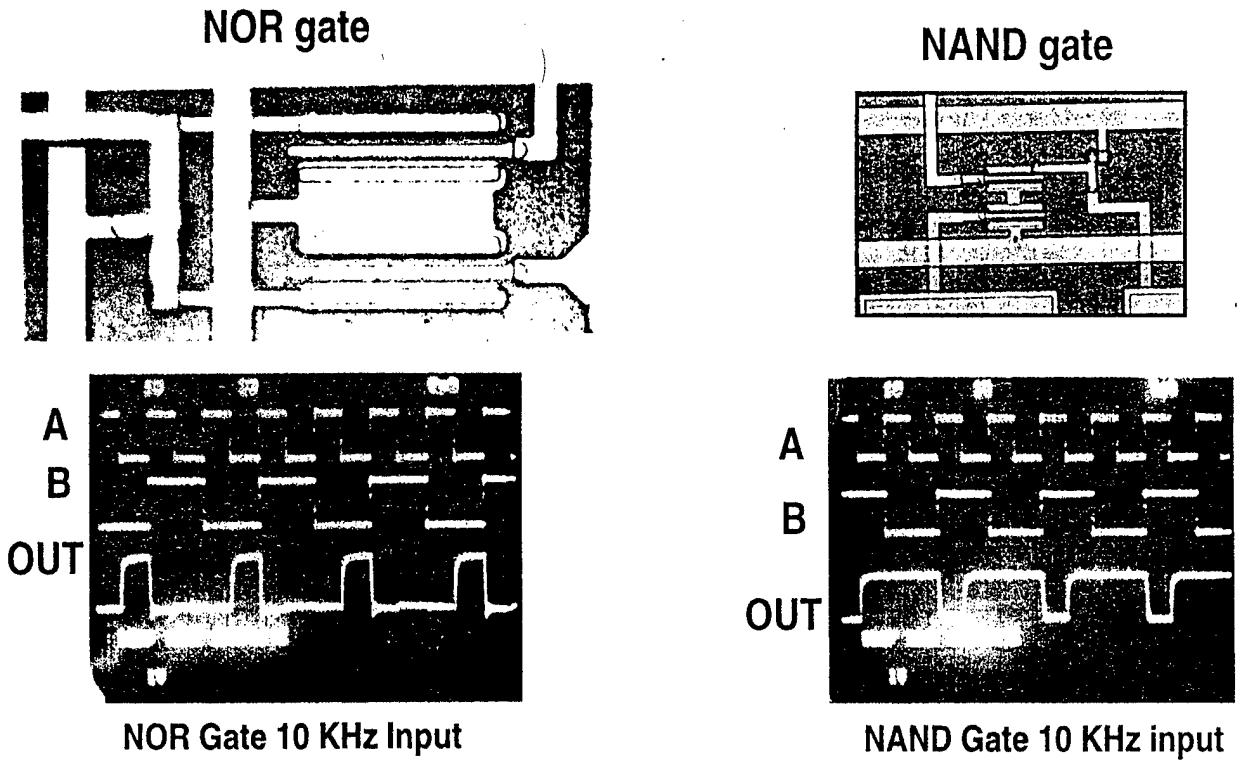
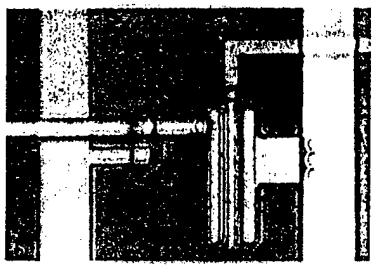
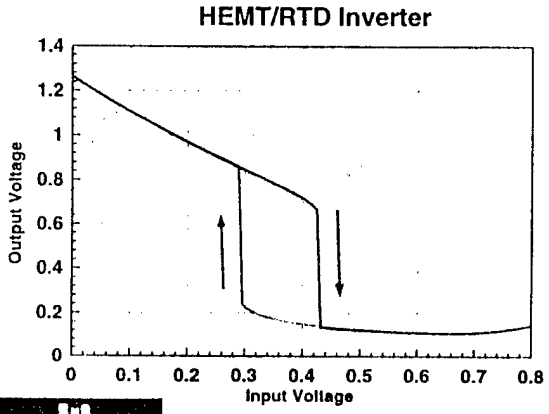


Fig. 39 Photo and output of properly functioning NOR and NAND Gates using lattice mismatched RTDs and HEMTs. This is the first demonstration of cointegrated InGaAs/AlAs RTDs with AlGaAs/GaAs HEMTs.



Inverter



Measured transfer curve

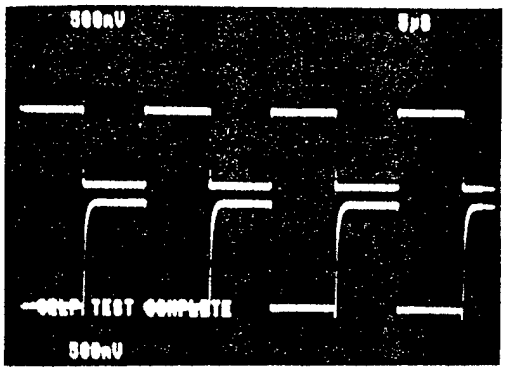


Fig. 40 Photo and output of properly functioning RTD/HFET inverter.

HEMT/RTD RUN SUMMARY

Lot Number/Wafer Number	HEMTs	RTDs
2A	Okay	4x4 PVCR=3.25
2D	Okay (Vt=0.2)	No RTDs
2E	Okay, Not uniform	some 4x4, PVCR=1.4
2G	Okay	Some 5x5, Low PVCR
2H	Good	Very low PVCR
3C	No HEMTs	3x3's okay, PVCR=3 (LM)
3A	No HEMTs	Bad contact
3B	HEMTs okay	low PVCR, Ind. of size
3D	HEMTs okay	some 6x6's "okay"
4A	Okay	No RTDs

Analysis of Circuit Test Results

One inverter gate will not drive the other inverter gate when connected in cascade. The following observations were made when testing a single inverter. (Some of these observations are not related to the failure.)

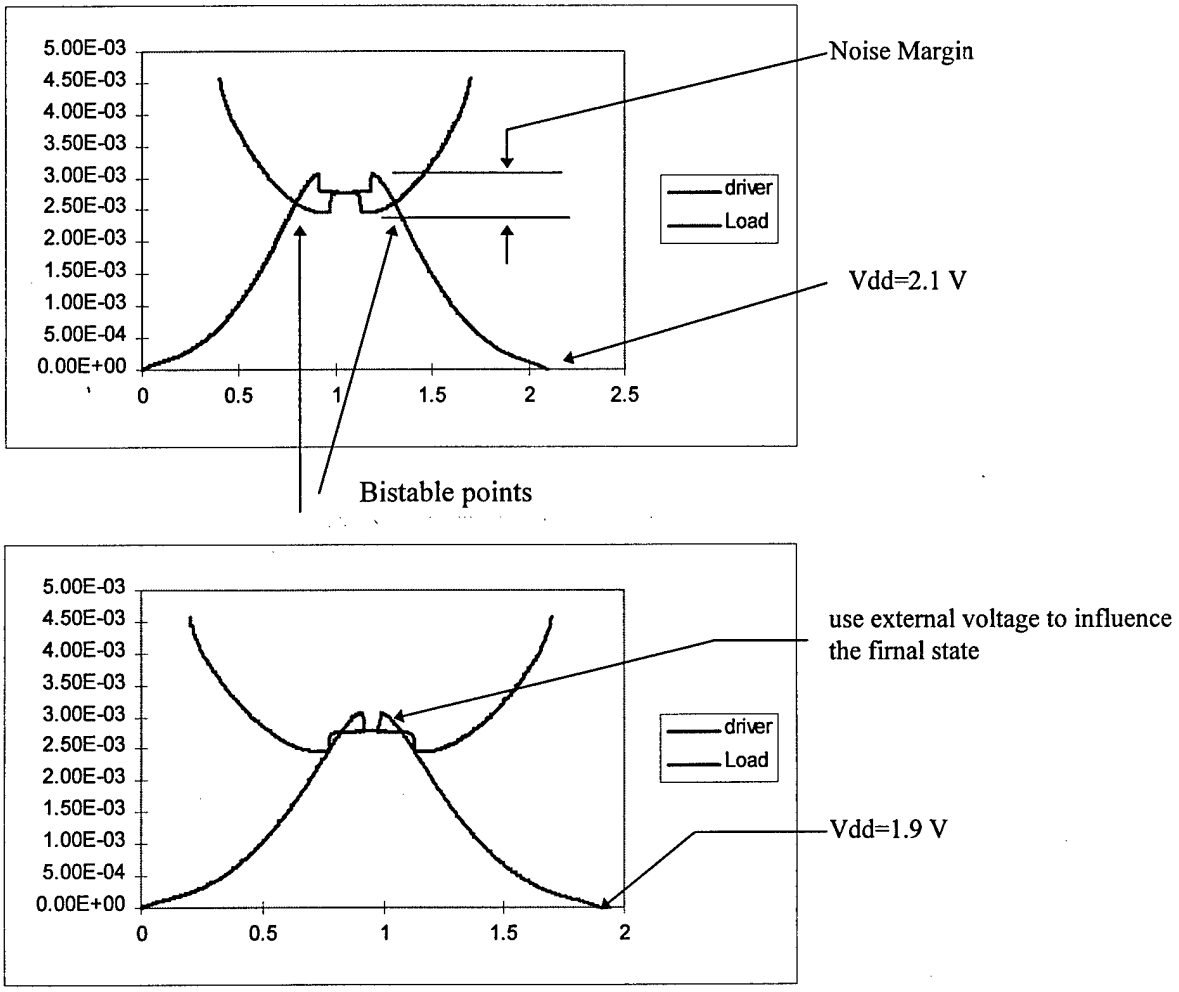
1. V_{dd} can be set anywhere between .9 to 1.8 to demonstrate single gate functionality. The higher the v_{dd}, the higher the V_{OH} will be.
2. V_{OL} is limited by the knee voltage of the HEMT near the I_d intersection with the RTD loadline. In our case, it is as low as 0.25 volt.
3. An input that switches from high (whatever that voltage may be) to 0.25 V will not be able to switch the output from low to high because V_{IL} (with the hysteresis effect) is around 0.2 V.
4. V_{OH} of these logic gates drops very quickly, for a slight increase of input voltage (the input voltage from external source starting at 0 volt). Possibly due to the high series resistance of RTDs.
5. As a result, in a ring of inverters all gates will remain at an output low. The means all RTDs are biased in the valley region, at a current of around 1.5mA for a 3 μm x 3 μm RTD. Since there are 19 stages plus two buffer stages, the overall current drawn from the source is about 21*1.5mA=31.5mA, which is close to what was measured.
6. By the same token, frequency dividers using the same family of logic will not work.

    Possible solutions:

    1. Increase V_{TH}. Difficult to do.
    2. Lower the knee voltage.

Explanation of RTD SRAM Failure

1. RTD SRAMs are bistable which can be explained from the following graph:



The bistable points are difficult to obtain because the noise margin are small. Higher PVR will help. V_{dd} swing from 2.1 to 1.9 V cannot be obtained from data generator, which is needed to generate synchronized signals that turn on gates, to allow data to be written to RTD pairs. So higher bias was used (1.9 to 2.4). This might also make the noise margin smaller.

6.0 LESSONS LEARNED

1) For lattice mismatched RTDs, need to reduce buffer layer thickness, due to yield and lithographic concerns.

2) Dry etch must be used for RTD definition. Particularly important for smaller area RTDs.

3) Similar programs should include a "tech development/modeling" mask so many material and process issues can be ironed out quickly.

4) RTD uniformity is still a critical issue, as is conventional device uniformity.

7.0 Conclusions

There were several key accomplishments of this program in developing technology for the monolithic integration of high quality RTDs and conventional III-V transistors such as HBTs and HEMTs. The first key accomplishment was the verification that HBT layers did not degrade during RTD growth cycle. This is a fundamental step for the demonstration of this technology. Working closely with Lincoln Lab, a process to fabricate RTDs at Rockwell was developed and RTDs with as drawn dimensions of 1.5x1.5, 2x2, 1.4x3, 5x5, and 3x1.4x8.5 μm^2 were demonstrated using ECR etching with a photo-resist mask. Lincoln Laboratory (LL) demonstrated a PVCR=9 lattice mismatched RTD on AlGaAs/GaAs HBT epilayers and the subsequent large area HBTs on this wafer were good. This is the first demonstration of co-integrated small area lattice mismatched RTDs and HBTs with a resulting RTD PVCR=9. An epitaxial design to provide improved emitter resistance and manufacturing tolerance by utilizing a low In concentration cap was demonstrated. This result has important implications for the manufacturability of HBTs in general.

Both AlGaAs/GaAs and InGaAs/AlAs RTDs were demonstrated on E/D HEMT material. This program provided the first demonstration of lattice mismatched RTDs with HEMTs. DCFL HEMT/RTD logic (inverter, NOR, and NAND) gates using the lattice mismatched material were also demonstrated.

There were a number of circuits designed and simulated in both HBT/RTD and HEMT/RTD technologies including: RI^2L: Multiple Fanout Gate, 17-Stage Ring Oscillator, 13 Stage Delay Chain, and requency divider. REHL: Full Adder, Multiple Fanout Gate, 17-Stage Ring Oscillator, 13 Stage Delay Chain; RTD/HFET Logic including shift-registers, small RAMs, logic gates, Frequency Dividers; REHL: Full Adder, Multiple Fanout Gate, 17-Stage Ring

Oscillator, 13-Stage Delay Chain; and RTD/HFET :Logic: including Shift Register, small RAMs, Logic Gates, Frequency Dividers, and Ring Oscillators.

We have developed the key buildingblocks of these technologies and demonstrated that lattice mismatched RTDs and conventional devices can be co-integrated. However, manufacturing issues such as reproducibility, reliability, mask c-factors, and device uniformity still need to be further explored before these technologies can be exploited for MSI and LSI circuits.

APPENDIX A

Models used in circuit simulations

BASELINE MODEL FOR GaAs RTD. 3x3 μm^2 Device.

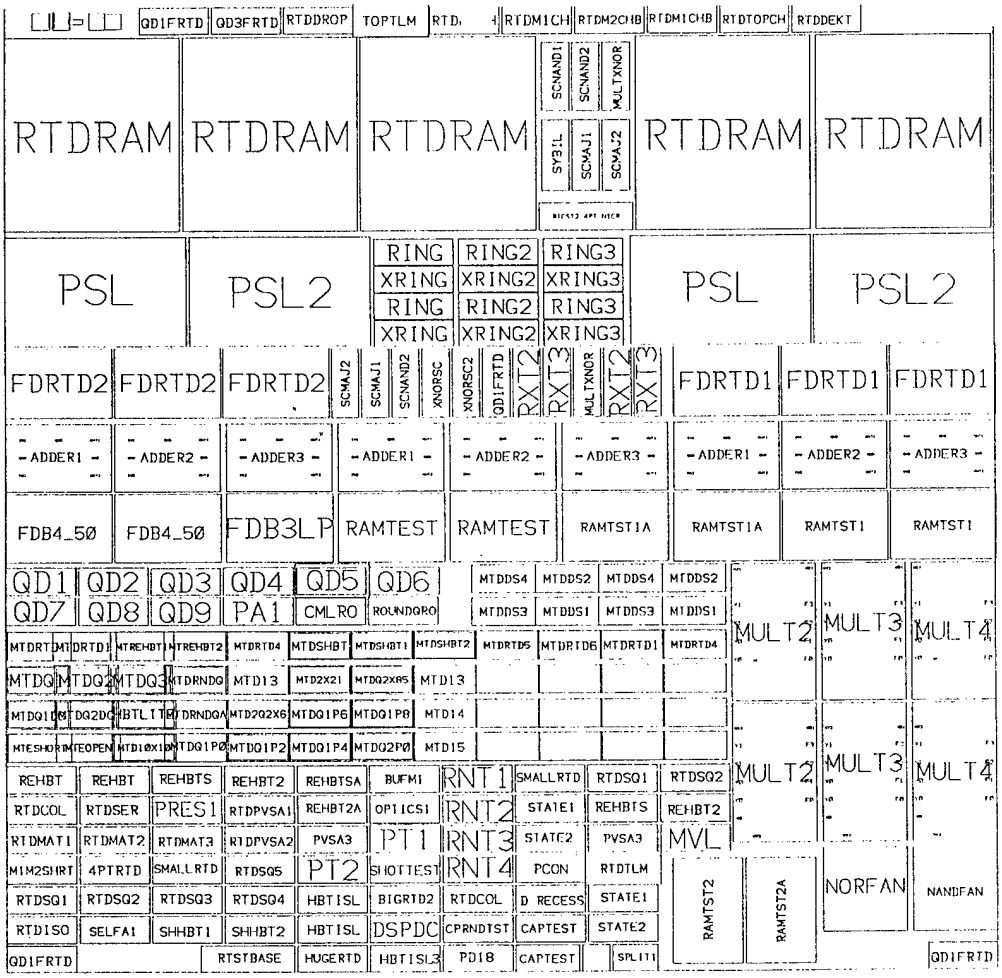
```
*circuit title - Baseline GaAs RTD model
.SUBCKT RTD 2 1
BRTDC 2 1 I=1.0*(0.001*(v(2)-v(1))*(atan(16.74*(v(2)-v(1))-6.5)-
+ atan(16.74*(v(2)-v(1))-13.0))+
+ 0.000244*(v(2)-v(1))+ 0.000078*(v(2)-v(1))^5)
DCAP 1 2 DIODE AREA=1.0
.MODEL DIODE D (is=1.0E-20 cjo=37.0ff vj=0.1)
*The I-V and C-V curves of the above models assume 9 square micron area
*as decided for the Lincoln Lab/Rockwell baseline RTD.  The
*RTD is assumed to have a peak current density of 2.0e4 A/cm**2 and
*a specific capacitance of 1.5 fF/square micron at the current peak.
.ENDS
```

BASELINE MODEL FOR InGaAs RTD. 3x3 μm^2 Device.

```
*circuit title - baseline InGaAs RTD model
.SUBCKT RTD 2 1
BRTDC 2 1 I=1.0*(0.0011*(v(2)-v(1))*(atan(16.74*(v(2)-v(1))-6.5)-
+ atan(16.74*(v(2)-v(1))-13.0))+
+ 0.000001*(v(2)-v(1))+ 0.000035*(v(2)-v(1))^5)
DCAP 1 2 DIODE AREA=1.0
.MODEL DIODE D (is=1.0E-20 cjo=37.0ff vj=0.1)
*The I-V and C-V curves of the above models assume 9 square micron area
*as decided for the Lincoln Lab/Rockwell baseline RTD.  The
*RTD is assumed to have a peak current density of 2.0e4 A/cm**2 and
*a specific capacitance of 1.5 fF/square micron at the current peak.
.ENDS
```

APPENDIX B

Contents of RH2GCA and RHIMS Mask Set



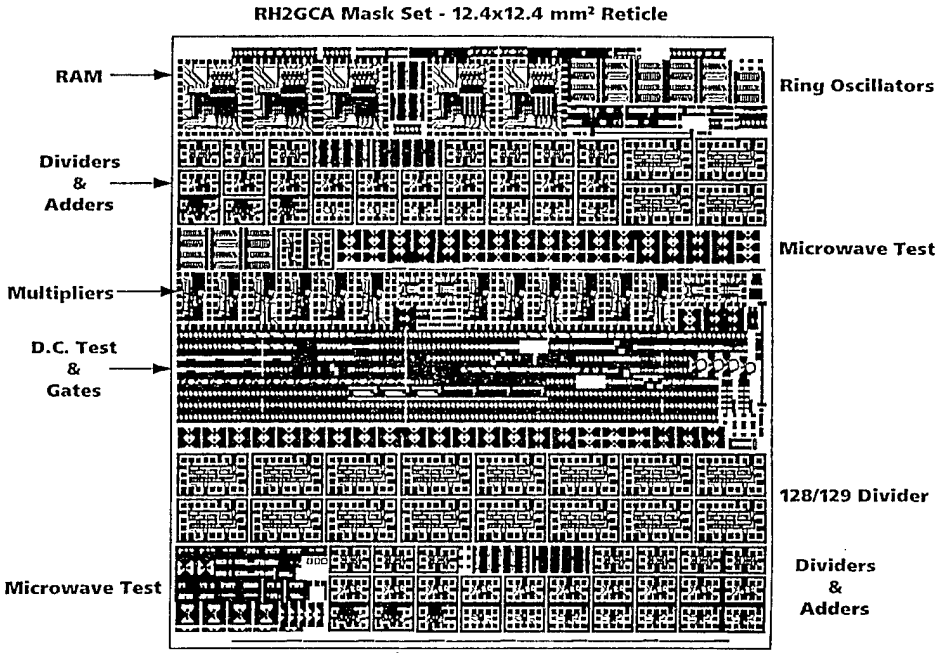


Fig. 28 RH2GCA Mask Set.

RTD/HBT Circuits:

ADDER1	REHL HBT/RTD Full Adder, 3x3 RTDs
ADDER2	REHL HBT/RTD Full Adder, 4x4 RTDs
ADDER3	REHL HBT/RTD Full Adder, 5x5 RTDs
CMLRO	11-stage CML ring oscillator, HBT Only
FDB3LP	HBT only divider, low power version
FDB4_50	HBT only divider, higher power, user friendly
fdrtd1	RTD frequency Divider (Divided by 4)
fdrtd2	RTD frequency Divide by 4
mult2	HBT/RTD multiplier, using TI architecture, 3x3 RTDs
mult3	HBT/RTD multiplier, 4x4 RTDs
mult4	HBT/RTD multiplier, 5x5 RTDs
psl	128/129 prescaler
psl2	128/129 prescaler
ring	RI2L NAND ring oscillator use 1.4x3um hbt and 80ff Cb
ring2	RI2L NAND ring oscillator use 1.4x6um hbt and 80ff Cb
ring3	RI2L NAND ring oscillator use 1.4x3um hbt and 50ff Cb
ROUNDQRO	11-stage CML RO with round transistors, HBT only
RTDRAM4	RTD/HBT static RAM
STATE1	State hold circuit, design 1
STATE2	State hold circuit, design 2
xring	REHL XNOR ring oscillator using 3x4 RTD
xring2	REHL XNOR ring oscillator using 3x3 RTD
xring3	REHL XNOR ring oscillator using 3x3 RTD with variation on load resistor

Logic Gates:

MULTXNOR	XNOR fan-out test
multxnor.cel	multiple xnor fanout (fanout=4)
MVL	1.4x6 HBT with area 1, 2, 4 RTDs on emitter (forward and reverse order)
NANDFAN	NAND gate fan-out test
NORFAN	NOR gate fan-out test
PA1	HBT differential pair
ramtest	
ramtst1	
ramtst1a	
RAMTST2	
RAMTST2A	
rnt1	RI2L NAND testing (fanout=1)
rnt2	RI2L NAND testing (fan in=6)
rnt3	RI2L NAND testing (fanout=3)
rnt4	RI2L NAND testing (fanout=4)
rxt2	REHL XNOR testing (fanout=3)

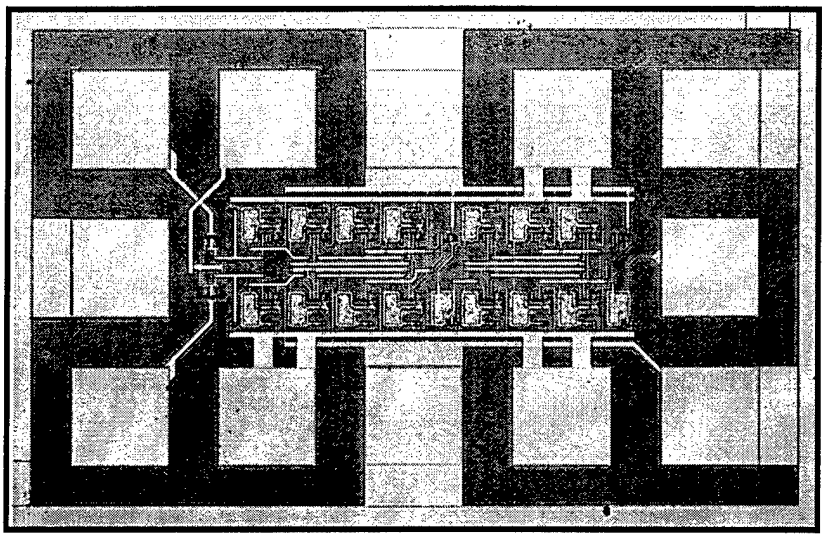
rxt3	REHL XNOR testing (fanout=1)
SCMAJ1	majority logic gate, 3x3 RTD
SCMAJ2	majority logic gate, 4x4 RTD
SCNAND1	nand gates with 3x3 RTD
SCNAND2	nand gates with 4x4 RTD
SYBIL	multifunctional gate
XNORSC	XNOR gate, 3x3 RTD
XNORSC2	XNOR gate, 4x4 RTD

Test Structures:

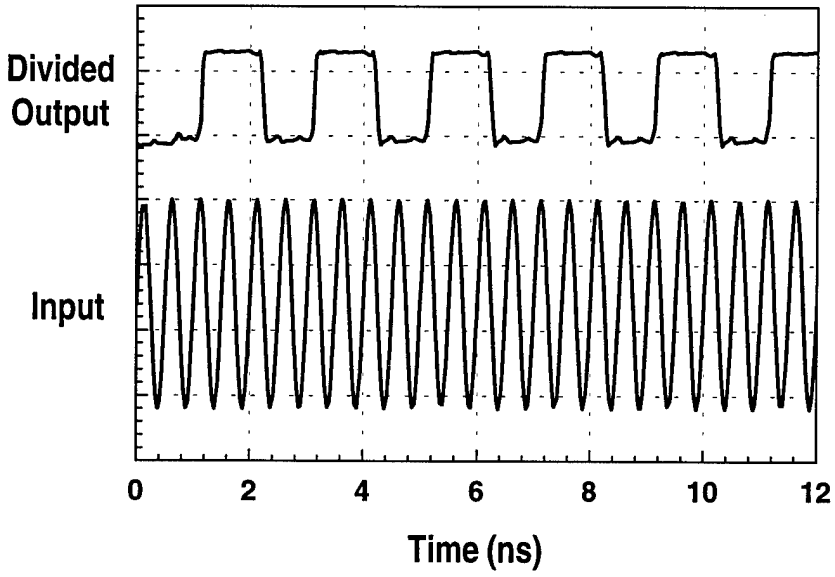
4PTRTD	Kelvin probeable RTD at m1 or m2
BIGRTD2	3x6, 12, 24, 48, 96, 192 double contact RTDs
BUFM1	Buffer layer test. Bottom to HBT emitter, RTD with HBT emit.
CAPRNDT	Round capacitor test
CAPTEST4	Small caps horizontal and vertical
CAPTST4B	Small caps, m2 horizontal
CRPCAP10	100x100 m2 defined
CRPCAP11	8 finger, 198.45x6.3 capacitor
CRPCAP6	Same as CRPCAP10 but mimv defined
CRPCAP9	Same as CRPCAP11, but mimv defined
DRECESS	Gate recess pattern for BiFET experiments
DSPDC	Series connected RTDs. M1 connected, double mesa, 2 double-mesas. 3x3 and 4x4 RTDs.
HBTISL	HBT inside RTD isolation box. Step from edge of box.
HBTISL2	HBT inside RTD bottom mesa box.
HBTISL3	HBT inside RTD top mesa box.
HBTLITE	HBT with no emitter metal inside
HUGERTD	185 4x4 RTDs
M1M2SHRT	M1 on bottom contact, M2 snaked over horizontally.
MTD10X10	10x10 HBT, microwave probe
MTD13	3x2x4 Schottky diodes
MTD14	3x2x8 Schottky diodes
MTD15	3x2x16 Schottky diodes
MTD2Q2X6	2 finger, 2x6 HBT
MTD2X21	2x2.1 HBT
MTDDS1	2 3x3 RTDs series connected with M1
MTDDS2	2 3x3 RTDs series connected through epi
MTDDS3	4 3x3 RTDs series connected. Epi & m2
MTDDS4	4 4x4 RTDs series connected Epi & m2
MTDQ1	1.4x3 HBT
MTDQ1DC	1.4x3 HBT, 2 collectors
MTDQ1P0	1.0x1.0 HBT
MTDQ1P2	1.2x1.2 HBT
MTDQ1P4	1.4x1.4 HBT
MTDQ1P6	1.6x1.6 HBT

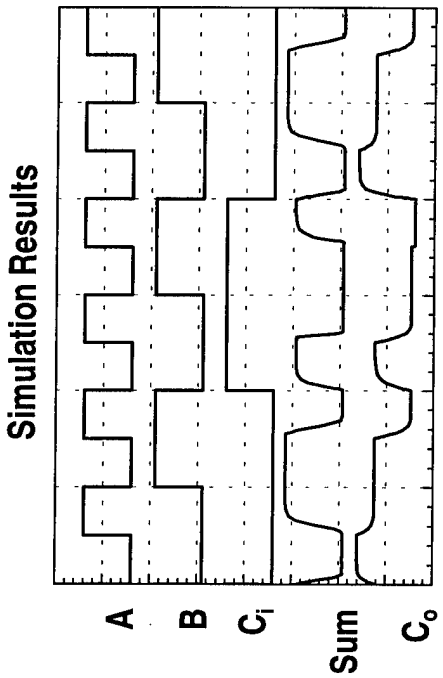
MTDQ1P8	1.8x1.8 HBT
MTDQ2	1.4x6 HBT
MTDQ2DC	1.4x6 HBT, 2 collectors
MTDQ2P0	2.0x2.0 HBT
MTDQ2X85	2x8.5 HBT
MTDQ3	3x1.4x8.5 HBT
MTDRNDQ	2.4 diameter HBT
MTDRNDQA	2.4 diameter HBT, round base
MTDRTD1	3x3 RTD
MTDRTD4	4x4 RTD
MTDRTD5	5x5 RTD
MTDRTD6	6x6 RTD
MTDSHBT	1.4x3 HBT with Schottky collector contact
MTDSHBT1	1.4x6 HBT with Schottky collector contact (will have bad yield)
MTDSHBT2	1.4x3 HBT with Schottky collector contact
MTEOPEN	Open for calibration
MTESHORT	Calibration short
MTREHBT1	1.4x3 HBT with 3x3 RTD on emitter
MTREHBT2	1.4x3 HBT with 3x3 RTD on emitter, large spacing
OPTICS1	RTD-light interaction experiments
PCON	BiFET p+ connection test.
PD18	Large m1/m2, mimv, and m2/m3 cap test
PRES1	base layer resistor test
PT1	Schottky diodes: single; 30 parallel, large
PT2	Diodes, various sizes with 1 and 2 contacts
PVSA3	3x3, 2x4.5, 2.5x3.6, 5x5, 3x8.33, 2.5x10
QD1	1.4x3.0 HBTs, 4pt 3x3 RTD, 10x10 RTD
QD1FRTD	3, 3, 4, 5, 6, 7 μm^2 RTDs probeable at M2
QD2	Q1, schottky diode, Q3, Qem (1.4 um x 50 um emitter for electron migration); single base HBT
QD3	Q1 split; Q3 split
QD3FRTD	Split RTD pattern for measuring resistances
QD4	Pads on GaAs: Q1, Q3; on SiO Q1, Q1B, Q1C
QD5	Q1E, Split B; Q1F, split B
QD6	1x1, 1x3, 1x24, 1.2x2 C, 1.2x2 A
QD7	1.4x1.4, 1.4x2, 1.4x6, 1.4x12, 1.4x24um
QD8	2x3, 2x24, 3x3, 3x24, 5x5um
QD9	Q2C14240, Q2E20120, Q100100, Q7070
REHBT	RTDs integrated into HBT emitter
REHBT1A	Small RTDs integrated into HBT emitter
REHBT2	Discrete HBT/RTD emitter, various spacings(6-9)
REHBT2A	Same as REHBT2 with center node access
REHBTS	Discrete HBT/RTD emitter, various spacings(2-5)
REHBTSA	Same as REHBTs with center node access
RTDCOL	0 to 10 um RTD-HBT collector spacing to bottom of RTD

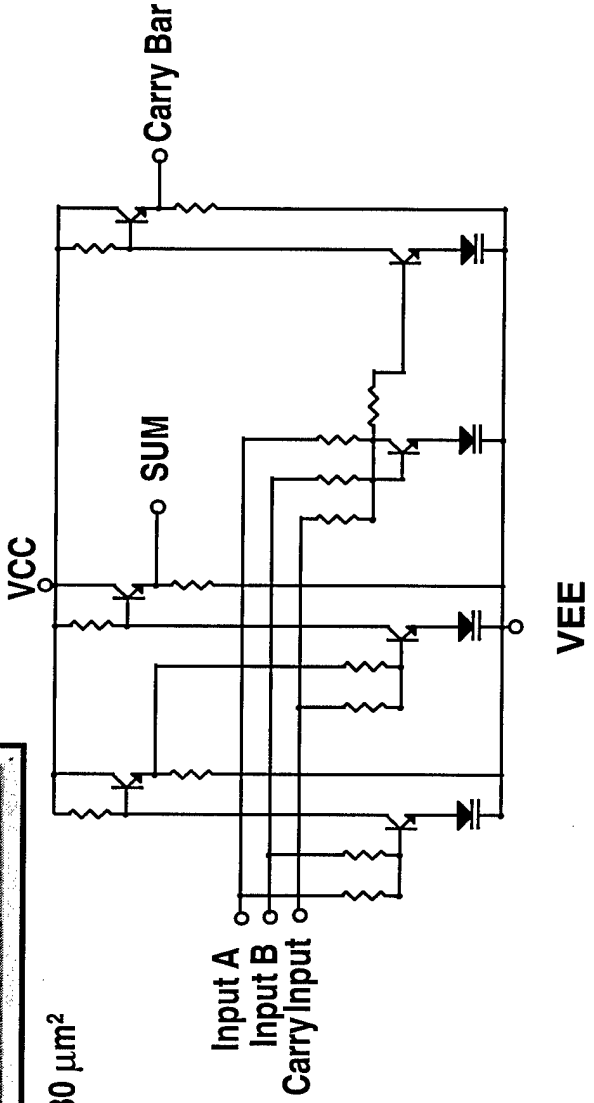
RTDDEKT	DEKTAK for RTD steps
RTDDROP	Drop in to measure resistivity for etch to bottom contact/em
RTDISO	RTD isolation experiments
RTDM1CH	4x4 RTDs with M1 snake
RTDM1CHB	M1 snake only
RTDM2CH	4x4 RTDs with M2 snake over
RTDM2CHB	M2 snake only
RTDMAT1	1-5 um RTD-RTD on bottom to top spacing
RTDMAT2	1-5 um RTD-RTD on top to top spacing
RTDMAT3	Shared contact matching test
RTDPVSA1	30x30, 90x10, 45x20, 50x18, 60x15, 75x12
RTDPVSA2	100x9, Round r=16.93
RTDSER	various RTD, schottky series/parallel combos
RTDSQ1	2,3,4,5,6,7 um2 devices, single contact
RTDSQ2	8,9,10,15,20,25 um2 devices, single contact
RTDSQ3	2,3,4,5,6,7 um2 devices, double contact
RTDSQ4	2,3,4,5,6,7 um2 devices, m1 single contact
RTDSQ5	2,3,4,5,6,7 um2 devices, m1 single contact
RTDTLM1	Top and bottom contact TLM
RTDTOPCH	M1 snake over top pedestal
RTEST2	nicr resistor test, 30x30, 30x3, 3x3, 3x30
RTHBT1	
RTHBT2	
RTHBT3	
RTHBT4	
RTHBT5	
RTHBT6	
RTSTBASE	base layer resistance test
SELFA1	self-aligned RTD experiments
SHHBT1	schottky-HBT DC test
SHHBT2	schottky-HBT DC test
SHOTTEST	schottky diode test
SMALLRTD	small area RTDs
SPLIT1	Split emitter HBT
TOPTLM	Top and bottom contact TLM

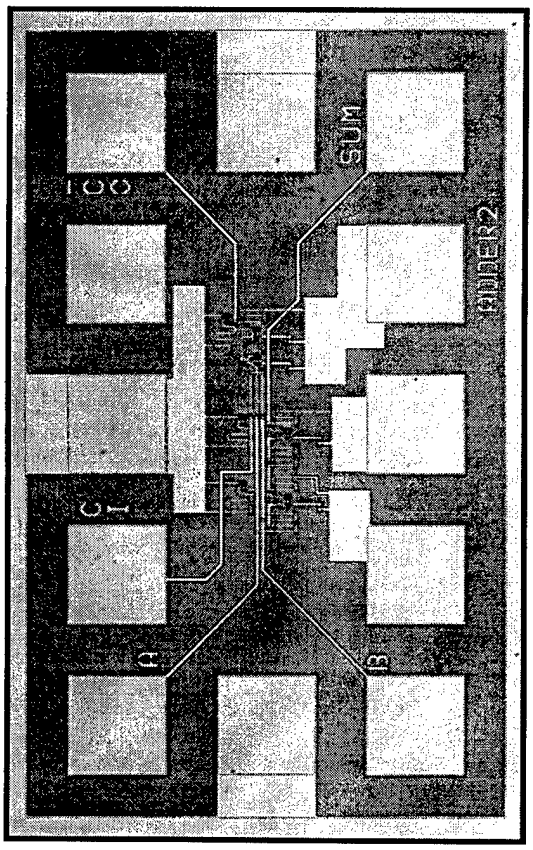


880x580 μm^2

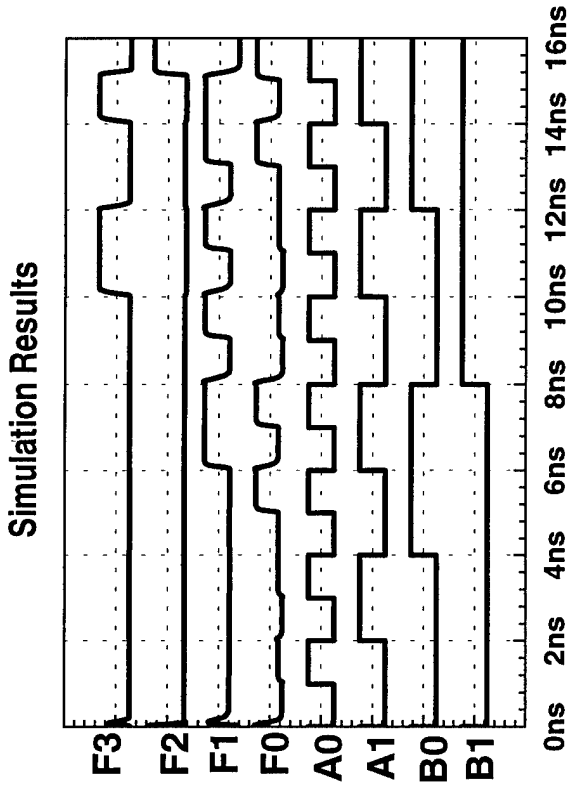


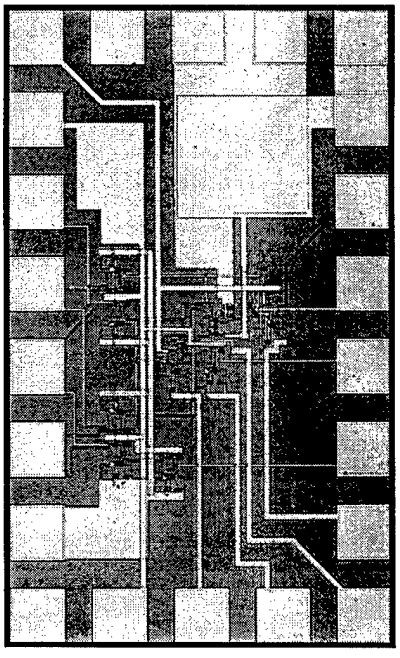

Simulation Results
A
B
C_i
Sum
C_o


Carry Bar
SUM
VCC
VEE
Input A
Input B
Carry Input

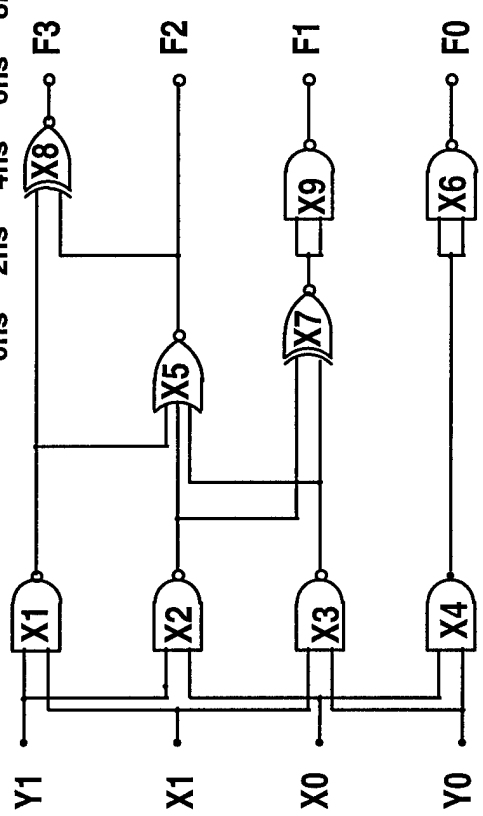

SUM
VCC
A
B
C_i

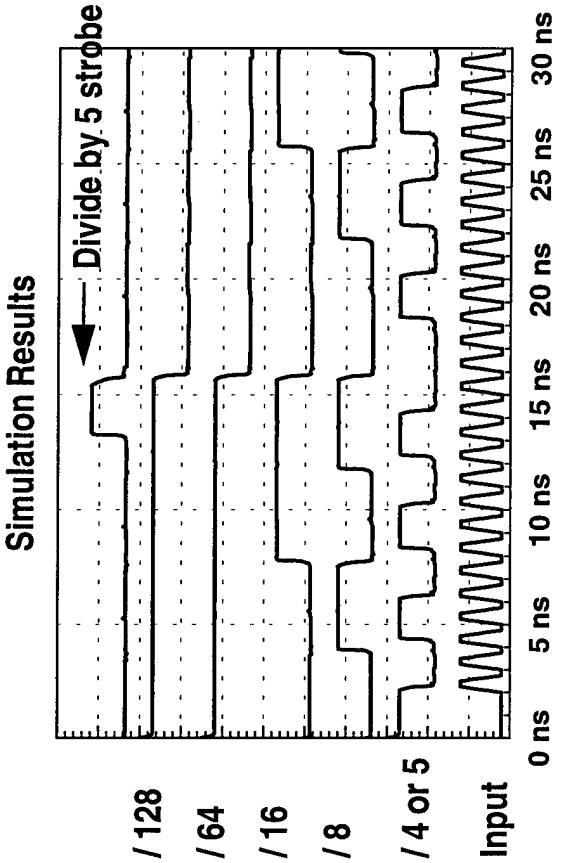
880x580 μm²

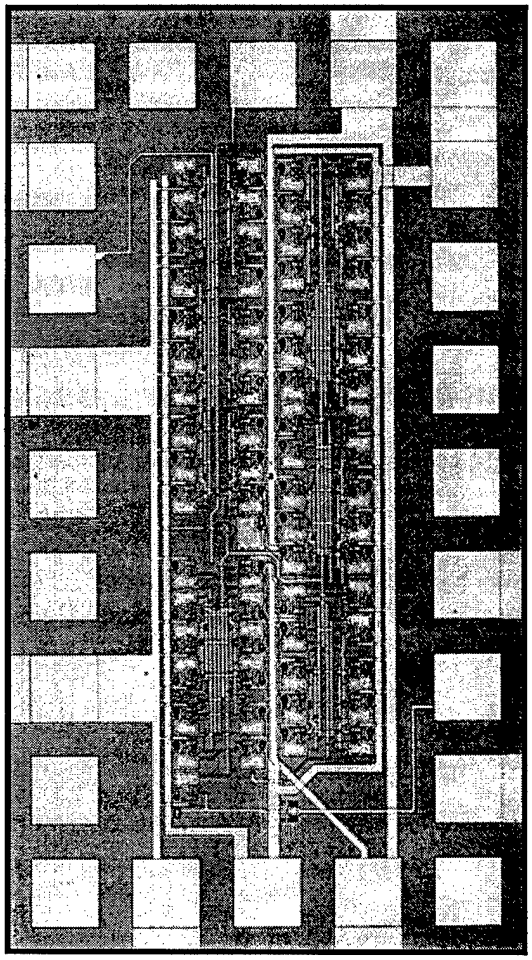


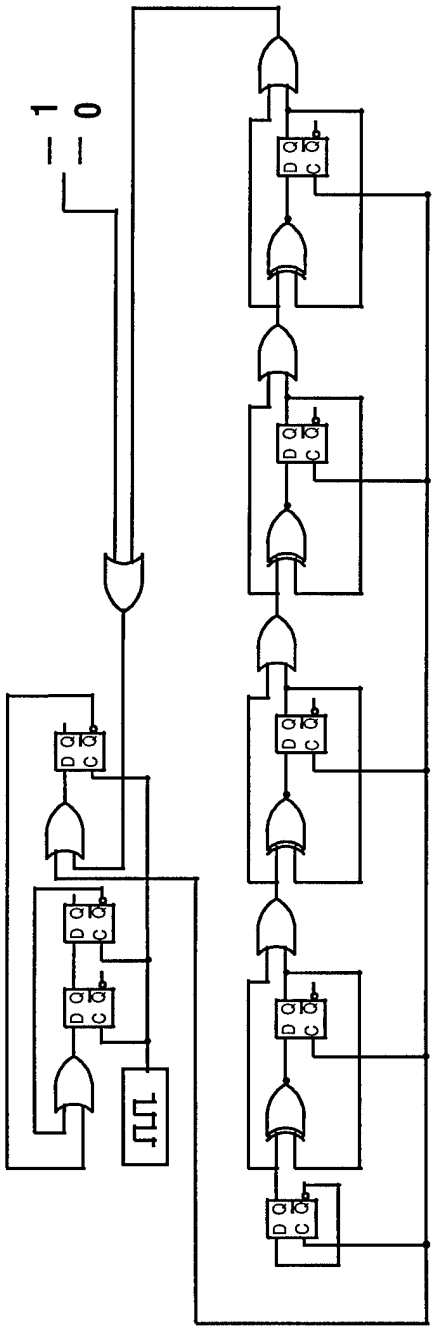


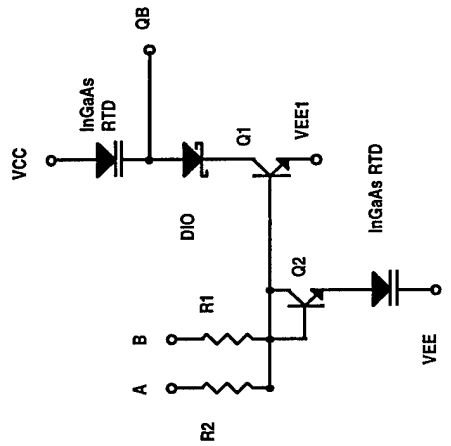
700x1500 μm²

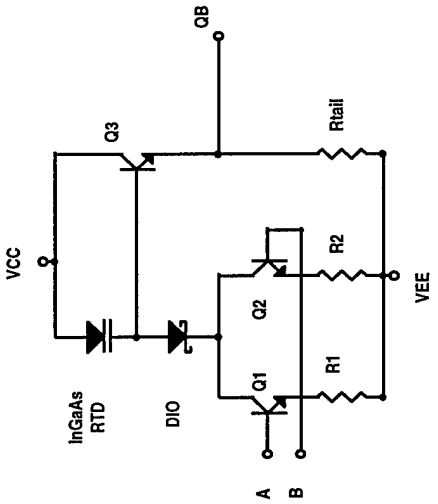


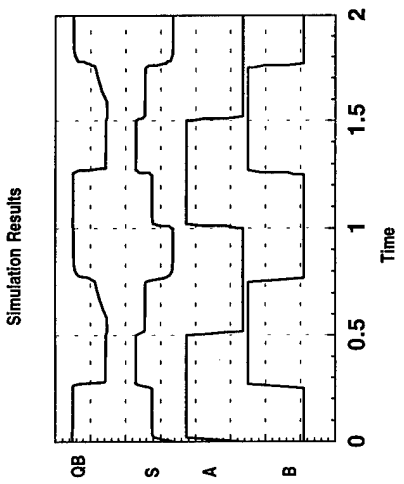

Simulation Results
Divide by 5 strobe
0 ns
5 ns
10 ns
15 ns
20 ns
25 ns
30 ns
Input
/ 4 or 5
/ 8
/ 16
/ 64
/ 128

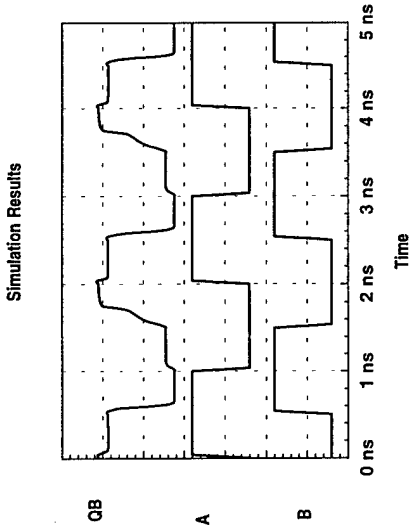


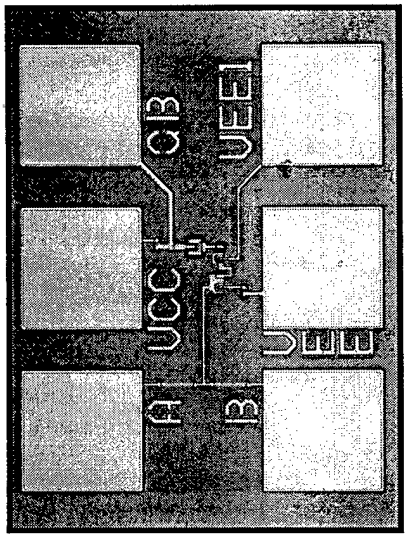

1
0



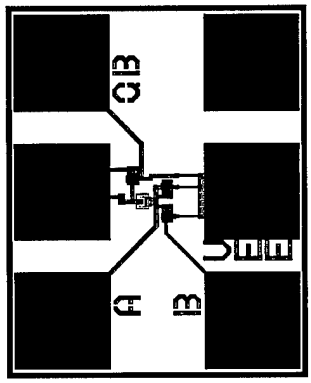








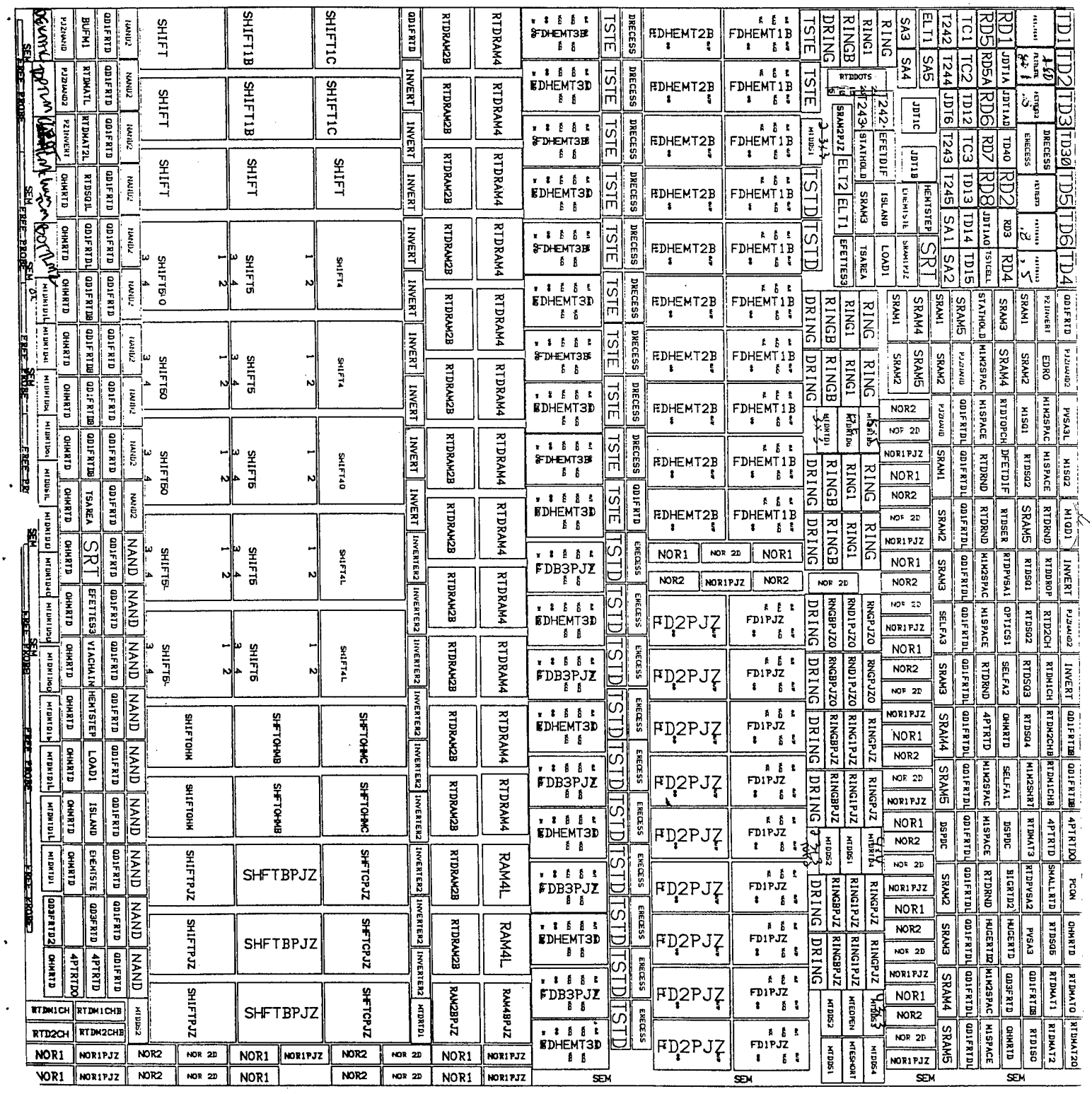
275x225 µm²



275x225 µm²

APPENDIX C

Contents of HR1MS Mask Set



HEMT/RTD Mask Set	
Most of the HEMT test structures were taken from ONR5 and ONR3 mask sets	
The RTD structures were taken from HR1DATA (HBT/RTD Mask Set)	
L Version = 2 um top to bottom contact spacing	
O Version = Ohmic metal used for RTD bottom contact	
CHIP NAME	Description
4PTRTD	Four Point Probeable RTD
4PTRTDL	Four Point Probeable RTD
4PTRTDO	Four Point Probeable RTD
BIGRTD2	Large Area RTDs
BOTTLM	TLM Probeable with 33 defined metal
BOTTLM2	Same as BOTTLM with ohmic bottom
BUFM1	Buffer layer experiments
CHANTLM	FET Channel TLM
DFETDIF	D-FET Differential Pair
DRECESS	D-HEMT Recess Pattern
DRING	Ring Oscillator using D-HEMT
DSPDC	DC Pattern series connected RTDs
EDRO	E-D HEMT Ring Oscillator
EFETDIF	E-FET Differential Pair
EFETTES3	staggered e devices from edge
EHEMTSTE	linear spacing e devices from edge
ELT1	horizontal FETs separated by an electrode
ELT2	vertical FETs separated by an electrode
FD1PJZ	Frequency divider, different RTD layout
FD2PJZ	Frequency divider, different RTD layout
FD3PJZ	Frequency divider, different RTD layout
FDHEMT1B	HEMT/RTD Divide by 4
FDHEMT2B	HEMT/RTD Divide by 4
FDHEMT3B	HEMT/RTD Divide by 4
FDHEMT3D	HEMT/RTD Divide by 4
FETTEST2	RF Test, DFET, 80x0.5
FETTEST3	RF Test, DFET, 80x0.8
FET_TEST	RF Test, DFET, 80x1.0
FETTESTE	RF Test, EFET, 80x1.0
FETTSTE2	RF Test EFET, 80x0.5
FETTSTE3	RF Test EFET, 80x0.8
HEMTSTEP	D FET loads
HUGERTD	185 4x4 RTDs in parallel
HUGERTD2	185 4x4 RTDs in parallel, m2 covered
INVERT	HEMT/RTD Inverter
INVERT2	E-D HEMT Inverter
ISLAND	HEMTs in RTD mesa box
JDT1A	FET Channels, Van der pol, EFET
JDT1AD	Same as JDT1A, for DFETs
JDT1AO	Same as JDT1AD
JDT1B	D Fat FET
JDT1C	E Fat FET
JDT6	Various width DFETs

LOAD1	D FET loads
M1M2SPAC	M1-M2 Spacing Test for RTD Yield
M1QD1	Top-Bottom spacing probeable at bottom contact
M1SPACE	m1 to m2 spacing check
M1SQ1	bottom contact probeable squares, 2-7 per side
M1SQ2	bottom contact probeable squares, 8,9,10,15,20,25 sides
MTDDS1	2 series integrated 3x3's in butterfly pattern
MTDDS1L	same as mtdds1, longer rtd
MTDDS2	2 series integrated 3x3's top contact only used
MTDDS3	4 series integrated 3x3's using only top contacts
MTDDS4	4 series integrated 4x4's using only top contacts
MTDRTD1	3x3 RTD Microwave Pattern
MTDRTD1L	3x3 RTD Long RTD Microwave Pattern
MTDRTD1O	3x3 RTD Ohmic bottom contact Microwave Pattern
MTDRTD1S	self-aligned 3x3 attempt
MTDRTD4	4x4 RTD Microwave Pattern
MTDRTD4L	4x4 RTD Long RTD Microwave Pattern
MTDRTD4O	4x4 RTD Ohmic bottom contact Microwave Pattern
MTDRTD5	5x5 RTD Microwave Pattern
MTDRTD5L	5x5 RTD Long RTD Microwave Pattern
MTDRTD5O	5x5 RTD Ohmic bottom contact Microwave Pattern
MTDRTD6	6x6 RTD Microwave Pattern
MTDRTD6L	6x6 RTD Long RTD Microwave Pattern
MTDRTD6O	6x6 RTD Ohmic bottom contact Microwave Pattern
MTDRTDLO	long with ohmic to bottom contact
MTEOPEN	Open for calibration
MTESHORT	Short for calibration
NAND	HEMT/RTD NAND Gate
NAND2	E-D HEMT NAND Gate
NOR1	HEMT/RTD NOR Gate
NOR1PJZ	Modified NOR1
NOR2	HEMT/RTD NOR Gate
NOR2D	HEMT/RTD NOR Gate
OHMRTD	Same as QD1FRTD, except with ohmic bottom contact
OPTICS1	large RTD for light interaction experiments
PCON	BiFET pcon pattern
PJZNAND	dual gate NAND gate. 30 um FET
PJZNAND2	dual gate NAND gate. 30 um FET, RTD m1 shifted
PVSA3	3x3, 2x4.5,2.5x3.6, 5x5, 3x8.3, 2.5x10 RTDs
PVSA3L	long versions of pvsa3
PJZINVERT	inverters, increased m1-m2 spacing by 1/2 micron
QD1FRTD	3, 3, 4, 5, 6, 7 RTDs
QD1FRTDB	1/2 micron increase in m2-m1 spacing
QD1FRTDL	long version
QD3FRTD	Split RTD, 2 bottom contacts
QD3FRTD2	ohmic to bottom
QD3FRTDL	long version
RAM2BPJZ	ram with aggressive layout
RAM4BPJZ	ram with aggressive layout
RAM4L	larger top-bottom spacing
RD1	E gate recess
RD2	E gate recess, no isolation under interconnect

RD3	Really RD5
RD4	E, aligned & shifted gates
RD5	E FET DC Test
RD5A	same as RD5
RD6	D gate recess
RD7	Same as RD6, no isolation under interconnect
RD8	D FET DC Test
RING	HEMT/RTD Ring Oscillator
RINGPJZ	m2-m1 increased
RING1	HEMT/RTD Ring Oscillator
RING1PJZ	increased m1-m2 spacing
RINGB	HEMT/RTD Ring Oscillator
RINGBPJZ	HEMT/RTD Ring Oscillator
RNG1PJZO	ohmic bottom contact
RNGPJZO	ohmic bottom contact
RTDDEKT	dektak pattern
RTDDROP	drop in pattern for bottom contact etch
RTDISO	isolation experiment on RTD bottom contact level
RTDM1CH	m1 snake over bottom contact of RTD
RTDM1CHB	m1 only for RTDM1CH
RTDM2CH	m2 snake over top contact of RTD
RTDM2CHB	m2 only for RTDM2CH
RTDMAT1	RTD Differential pairs, top-bottom orientation
RTDMATL	long version of RTDMAT1
RTDMATO	ohmic version
RTDMAT2	RTD Differential pairs, top-top
RTDMAT2L	long version of RTDMAT2
RTDMAT2O	ohmic version
RTDMAT3	RTD Differential pairs, 1 bottom contact
RTDPVSA1	30x30, 10x90, 45x20, 50x18, 60x15, 75x12
RTDPVSA2	100x9, 300x3, Round
RTDRAM2B	2x2 RAM, Bits only
RTDRAM4B	4x4 RAM, Bits only
RTDRND	1.5, 2, 2.5, 3, 4, 5 Diameter RTDs
RTDSEM	RTD SEM Pattern, placed in both X and Y directions
RTDSER	2-3x3's, 3-3x3's, 3x3-4x4, 3x3-4x4-5x5, diff pair
RTDSQ1	2, 3, 4, 5, 6, 7 on side RTDs
RTDSQ1L	long version
RTDSQ2	8, 9, 10, 15, 20, 25 on side RTDs
RTDSQ2L	long version
RTDSQ3	3, 3, 4, 5, 6, 7 on side, two bottom contacts
RTDSQ4	2, 3, 4, 5, 6, 7 m1 only on contact
RTDSQ5	Same as RTDSQ4, larger spacing from m2-m1
RTDTLM1	TLM for process using top and bottom contacts as etch only
RTDTOPCH	m1 snake over RTD top
SA1	sense-amplifier
SA2	sense-amplifier
SA3	sense-amplifier
SA4	sense-amplifier
SA5	sense-amplifier
SELFA1	3, 3, 4, 5, 6, 7 on side self-aligned RTDs
SELFA2	3, 3, 4, 5, 6, 7 on side self-aligned RTDs, aggressive design

SELFA3	arrays of sizes for process probing				
SHIFT	HEMT/RTD Shift Register				
SHIFTOHM	ohmic version				
SHIFTPJZ	tighter layout version				
SHIFT1B	HEMT/RTD Shift Register				
SHFTBPJZ	tighter layout version				
SHFTOHMB	ohmic version				
SHIFT1C	HEMT/RTD Shift Register				
SHFTCPJZ	tighter layout version				
SHFTOHMC	ohmic version				
SMALLRTD	0.5, 0.7, 1.0, 1.3, 1.5, 1.7x1.5 RTDs				
SRAM1	HEMT/RTD RAM Cell				
SRAM1PJZ	tighter layout version				
SRAM2	HEMT/RTD RAM Cell				
SRAM2PJZ	tighter layout version				
SRAM3	HEMT/RTD RAM Cell				
SRAM4	HEMT/RTD RAM Cell				
SRAM5	HEMT/RTD RAM Cell				
SRT	Saturated Resistor Test				
STATHOLD	state-holding circuit, m1 probe, gate probe				
T242	D source-drain spacing				
T243	E source-drain spacing				
T244	E-D inverter				
T245	E-D inverter				
TC1	push-pull, HEMT only				
TC2	E-D NAND Gate, HEMT only				
TC3	DFET S.F. HEMT only				
TD1	E, gate width				
TD12	1x300 DFET				
TD13	1x300 EFET				
TD14	5x300 DFET				
TD15	5x300 EFET				
TD2	D, gate width				
TD3	E, gate length				
TD3O	E, orientation				
TD4	D, gate length				
TD4O	D, orientation				
TD5	E, asymmetry				
TD6	D, asymmetry				
TOPTLM	same as chantlm, except for TOP has via				
TSAREA	E FET Size				
TSTCELL	E-Diode Test				
TSTD	D-HEMT Test				
TSTE	E-HEMT Test				
VIACHAIN	Via chain test pattern				